MicroConverter®, Dual-Channel 16&24 bit ADCs with Embedded FLASH MCU

Errata Sheet — ADuC824

A. This Errata sheet represents the known bugs, anomalies and work-arounds for the ADuC824 MicroConverter.

B. The Errata listed, apply to all ADuC824 packaged material branded as follows :

ADUC824BS
Date Stamp AD Logo
Lot Number

C. Analog Devices Inc. is committed, through future silicon revisions to continuously improve silicon functionality. Analog Devices Inc. will use its best endeavors to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended work-arounds outlined in this document.

D. ADuC824 Silicon Errata Sheet Revision History :

Revision	Date :	Relevance	Silicon Status	# of Bugs Reported
1.0	Dec. `00	All Silicon branded ADUC824BS	Released	1 - 824_01

REV. 1.00 Dec.'00

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 # 824_01. INDIRECT ADDRESSING MODE- :

Background: In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.
eg. MOV A, @R0.

Issue: The following Special Function Registers (SFRs) cannot be read using indirect addressing modes: ADCMODE, ADC0CON, ADC1CON, SF, ICON, PSMCON, ADCSTAT, ADC0L/M/H, ADC1L/H, OF0L/M/H, OF1L/H, GN0L/M/H, GN1L/H, DACL/H, DACCON.

Work-Around : Instead of executing the indirectly addressed read instruction as
MOV @Ri, ADCSTAT
It should instead be executed as
MOV A, ADCSTAT
MOV @Ri, A

Related Issues : Reading, using indirect addressing, functions correctly for all SFRs other than those mentioned above.

Writing, using indirect addressing, functions correctly for all SFRs including those mentioned above.
