PRACTICAL DESIGN TECHNIQUES FOR SENSOR SIGNAL CONDITIONING

LOW POWER, LOW VOLTAGE ADC DESIGN ISSUES

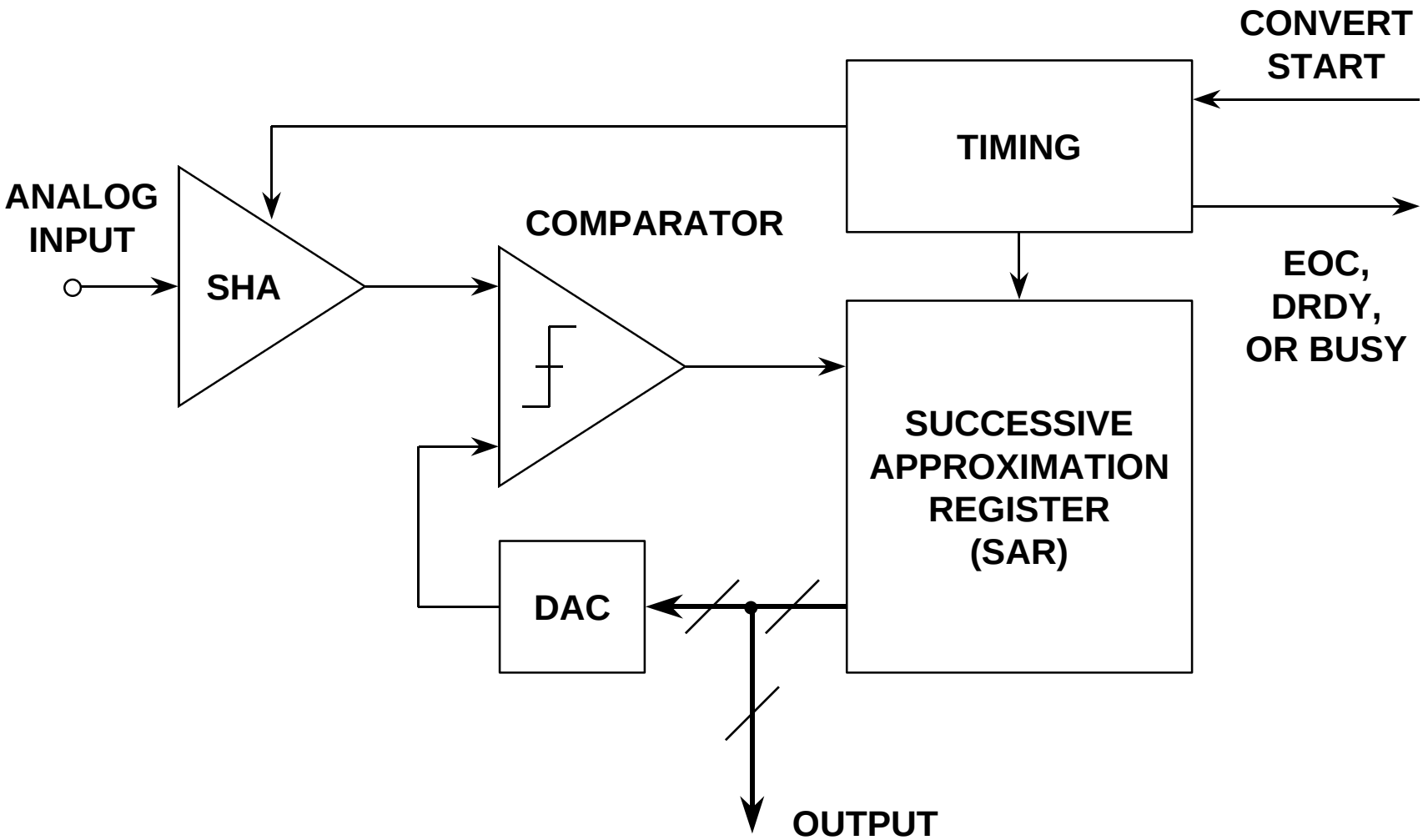
- **Typical Supply Voltages: ±5V, +5V, +5/+3V, +3V**
- **Lower Signal Swings Increase Sensitivity to**

  All Types of Noise (Device, Power Supply, Logic, etc.)
- **Device Noise Increases at Low Currents**
- **Common Mode Input Voltage Restrictions**
- **Input Buffer Amplifier Selection Critical**
- **Auto-Calibration Modes Desirable at High Resolutions**

ADCs FOR SIGNAL CONDITIONING

- **Successive Approximation**
  - **Resolutions to 16-bits**
  - **Minimal Throughput Delay Time**
  - **Used in Multiplexed Data Acquisition Systems**
- **Sigma-Delta**
  - **Resolutions to 24-bits**
  - **Excellent Differential Linearity**
  - **Internal Digital Filter, Excellent AC Line Rejection**
  - **Long Throughput Delay Time**
  - **Difficult to Multiplex Inputs Due to Digital Filter Settling Time**
- **High Speed Architectures:**
  - **Flash Converter**
  - **Subranging or Pipelined**

SUCCESSIVE APPROXIMATION ADC



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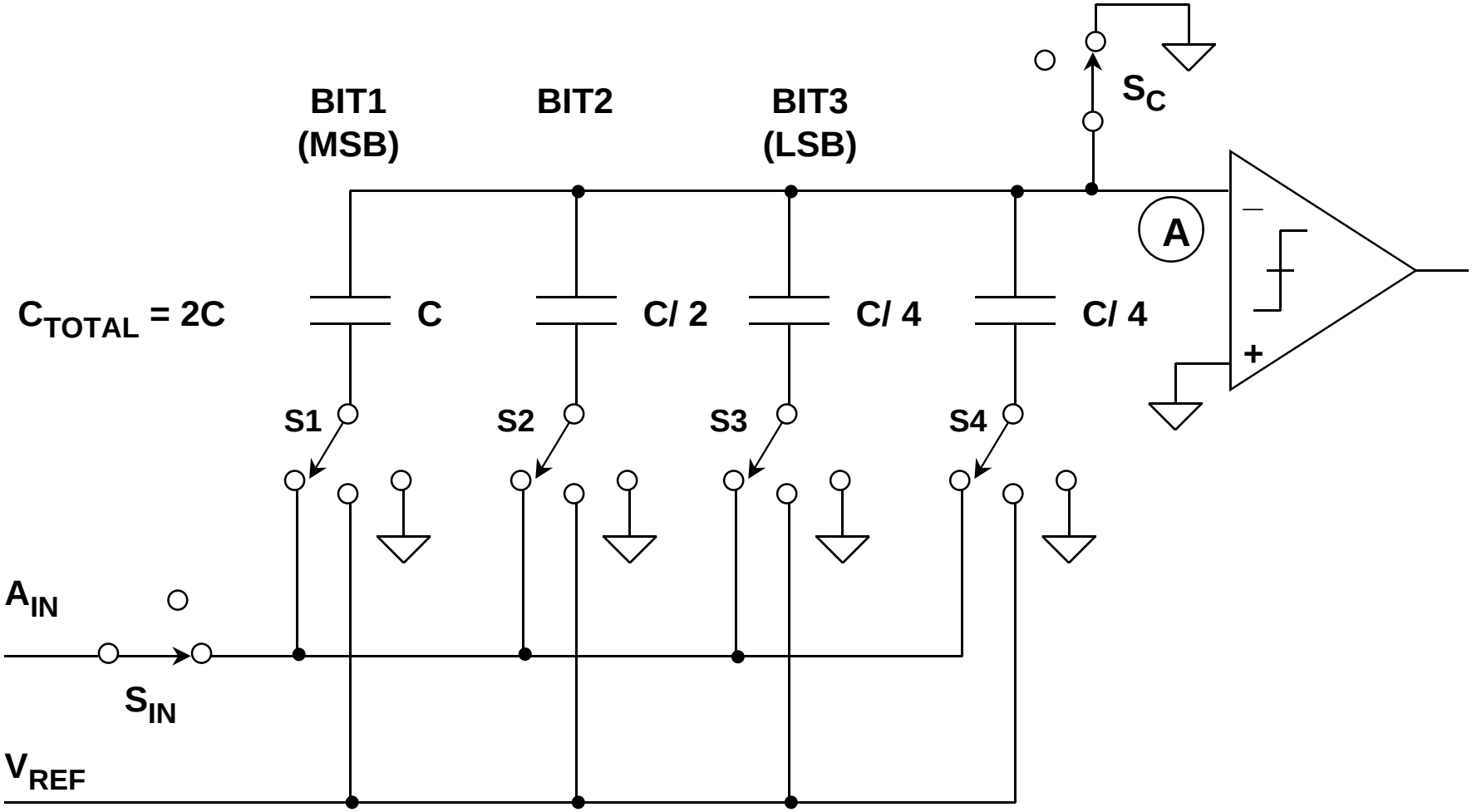
3-BIT SWITCHED CAPACITOR DAC



SWITCHES SHOWN IN TRACK (SAMPLE) MODE

a

RESOLUTION / CONVERSION TIME COMPARASION FOR REPRESENTATIVE SINGLE-SUPPLY SAR ADCs

	RESOLUTION	SAMPLING RATE	POWER	CHANNELS
AD7472	12-BITS	1.5MSPS	9mW	1
AD7891	12-BITS	500kSPS	85mW	8
AD7858/59	12-BITS	200kSPS	20mW	8
AD7887/88	12-BITS	125kSPS	3.5mW	8
AD7856/57	14-BITS	285kSPS	60mW	8
AD974	16-BITS	200kSPS	120mW	4
AD7670	16-BITS	1MSPS	250mW	1

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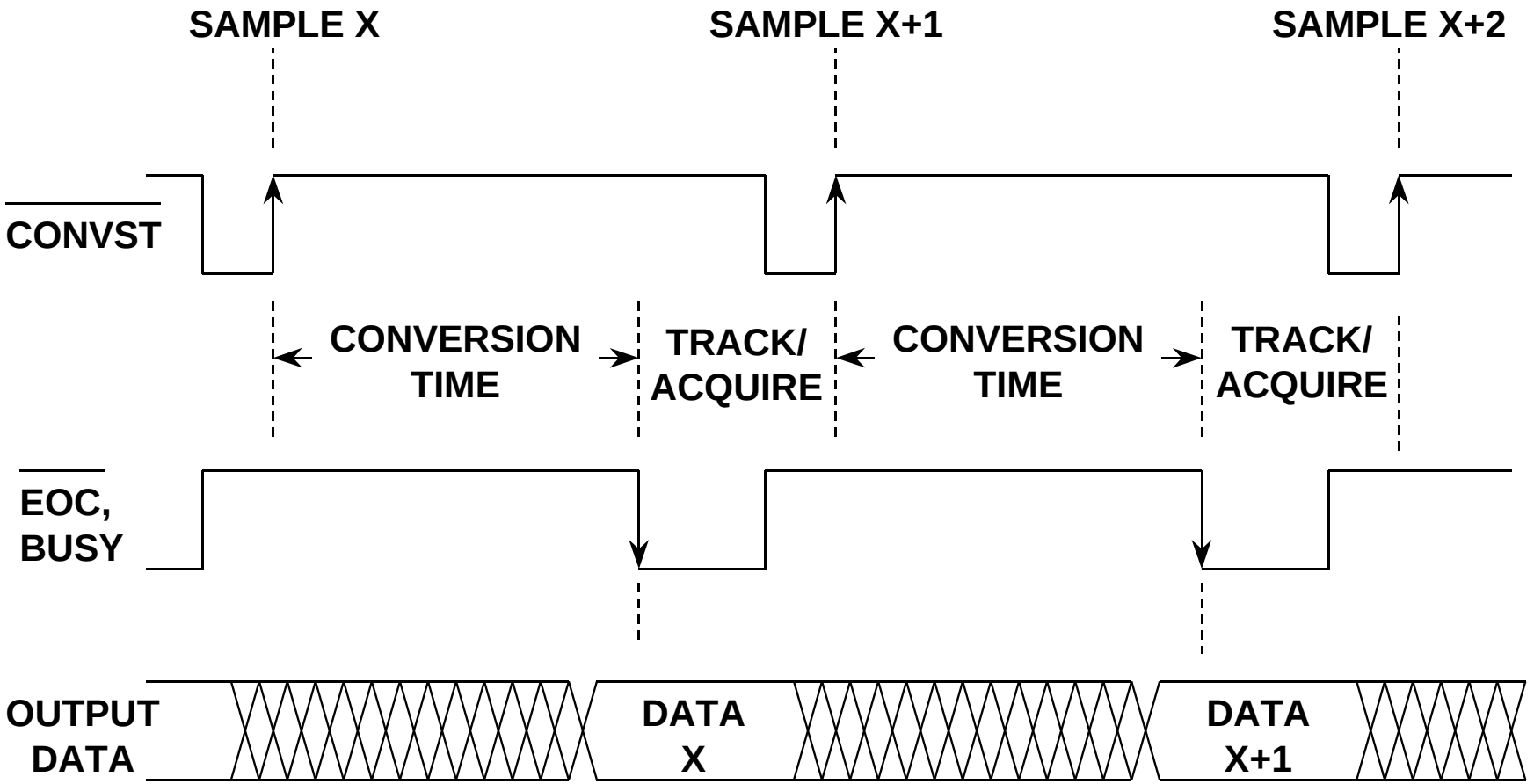
TYPICAL SAR ADC TIMING



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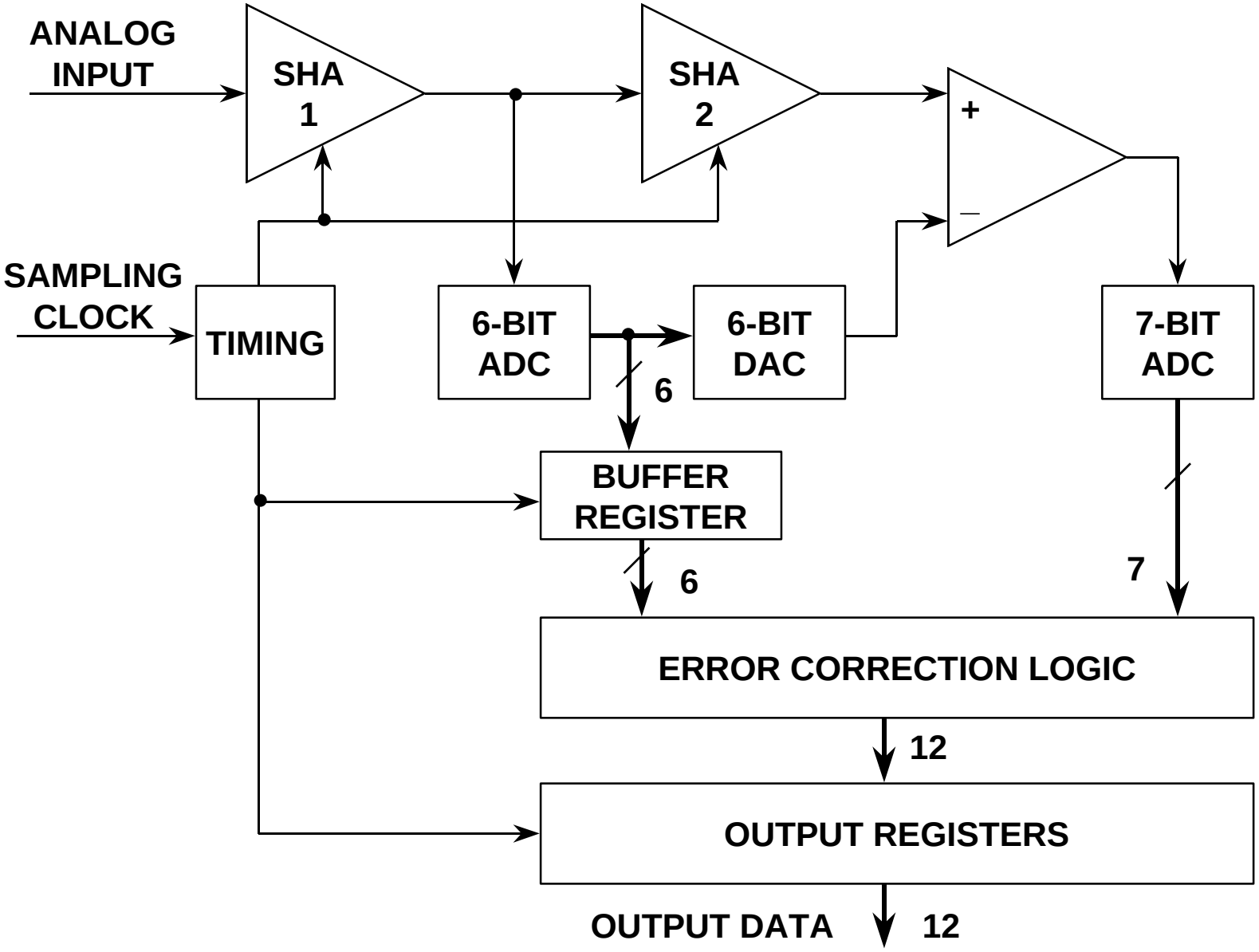
12-BIT TWO-STAGE PIPELINED ADC ARCHITECTURE



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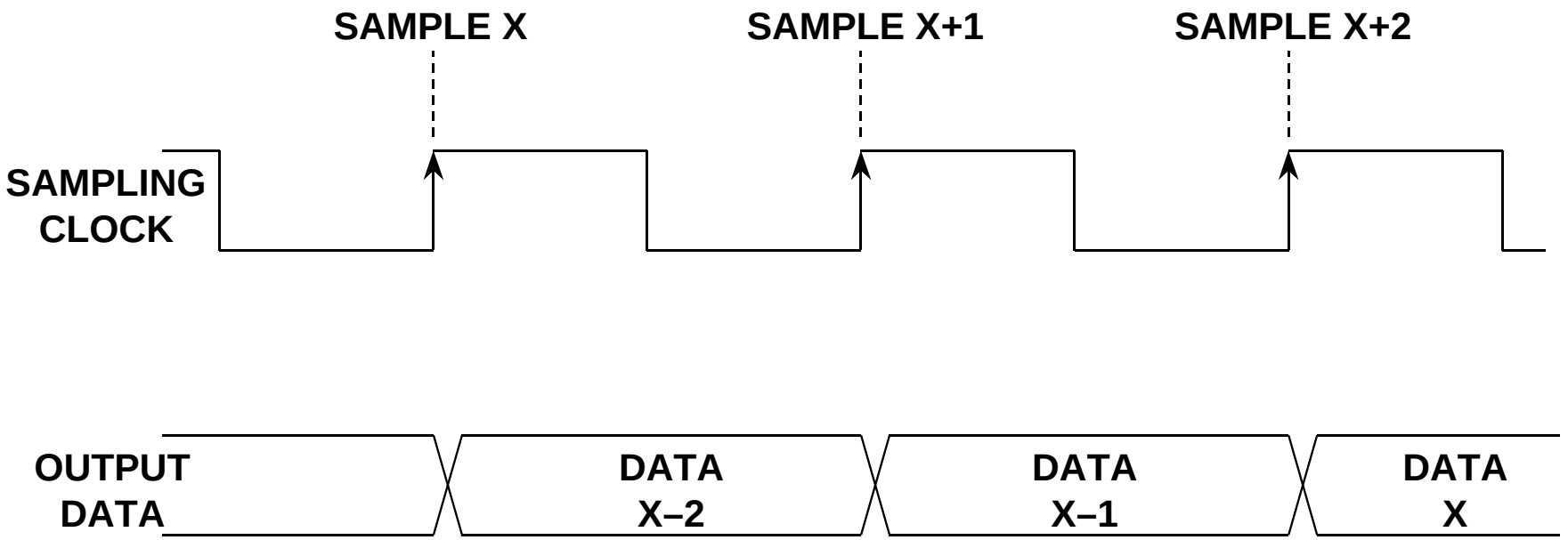
TYPICAL PIPELINED ADC TIMING



ABOVE SHOWS TWO CLOCK-CYCLES PIPELINE DELAY

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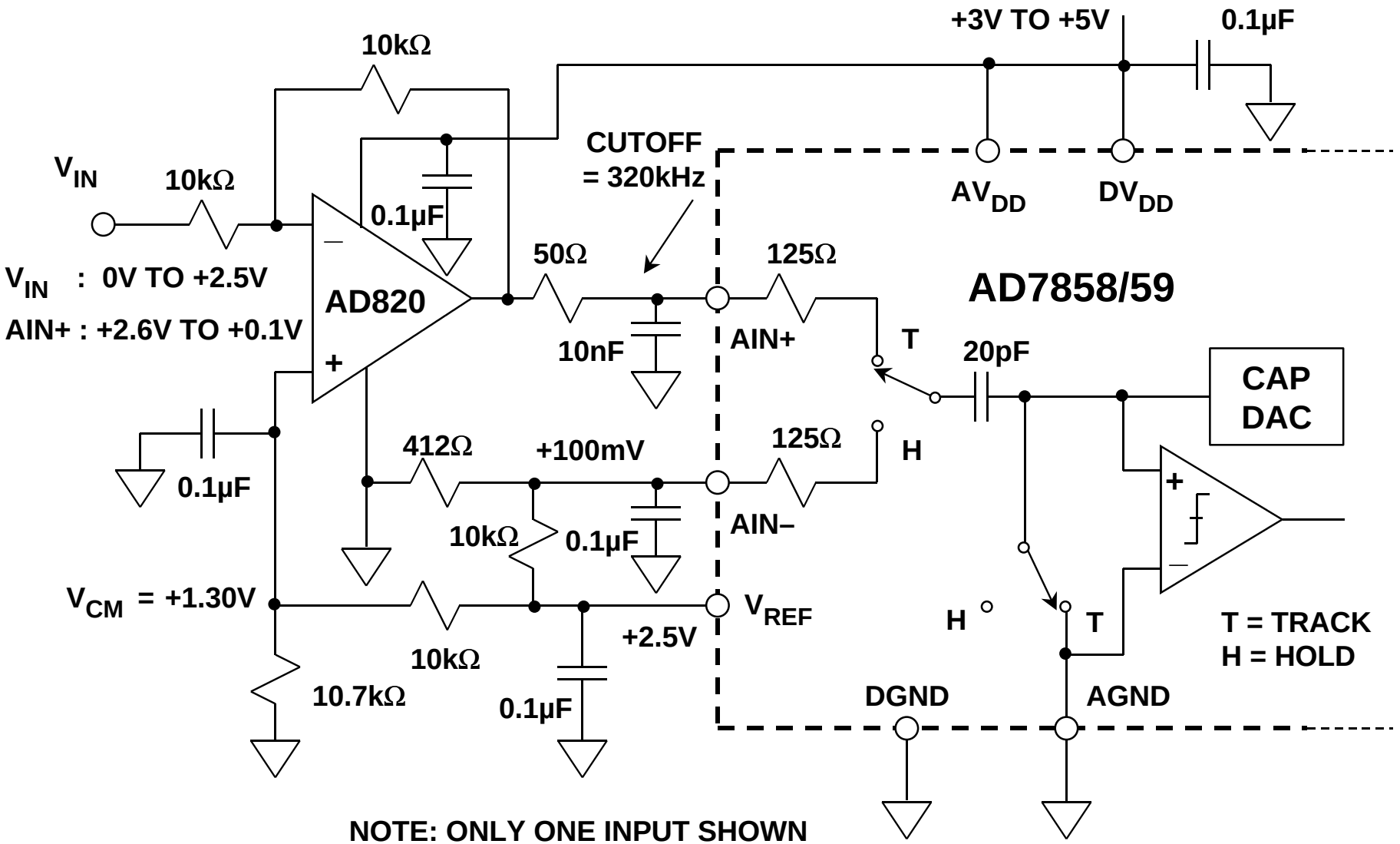
DRIVING SWITCHED CAPACITOR INPUTS OF AD7858/59 12-BIT, 200kSPS ADC



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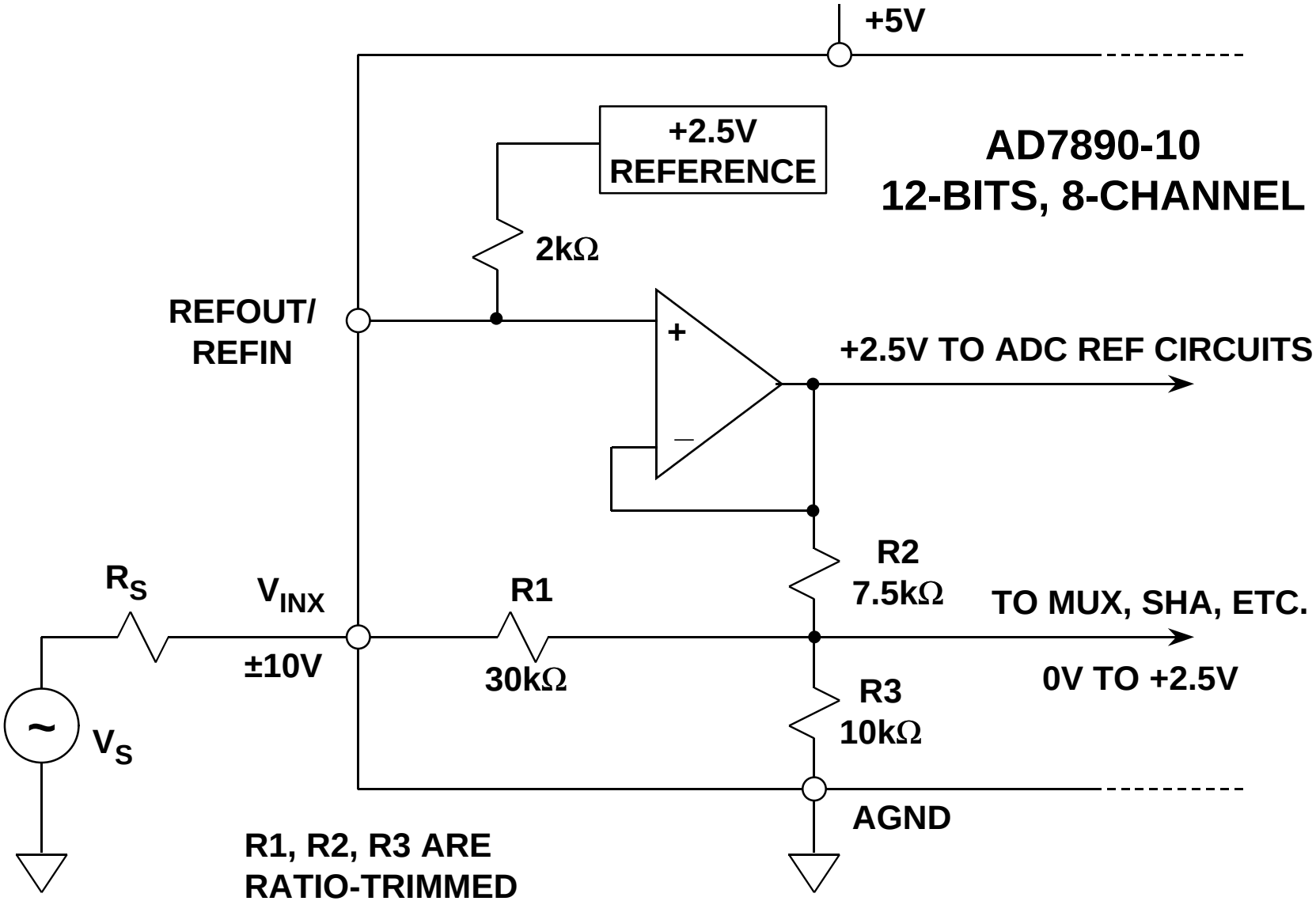
DRIVING SINGLE-SUPPLY ADCs WITH SCALED INPUTS



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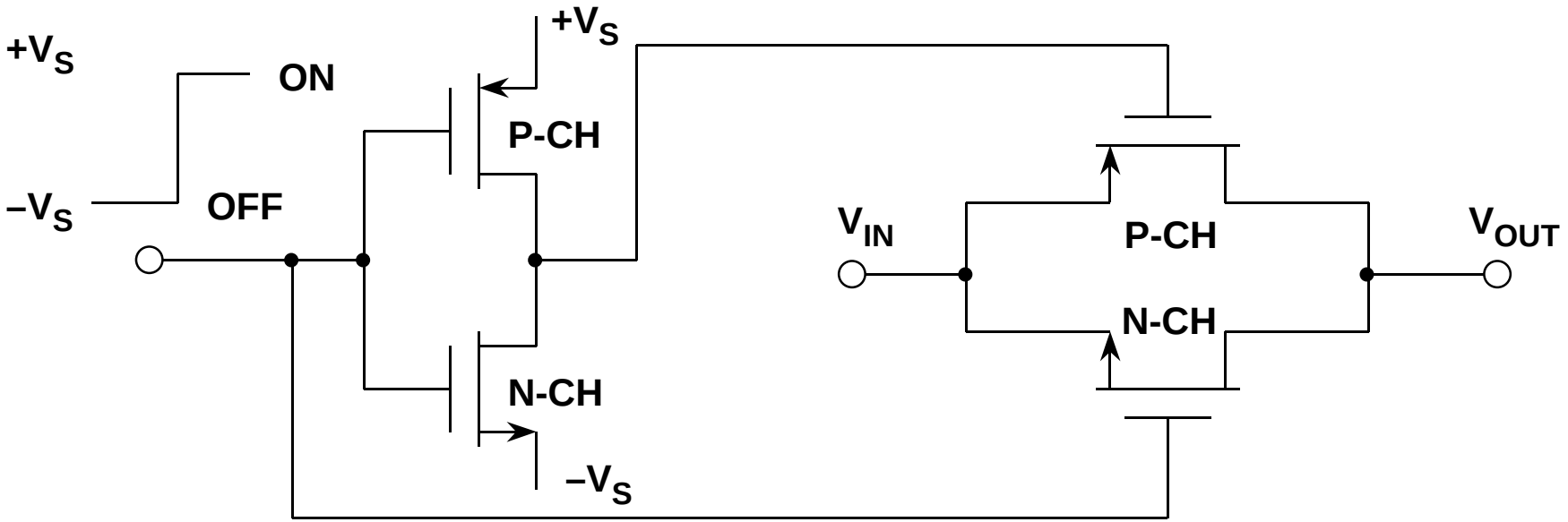
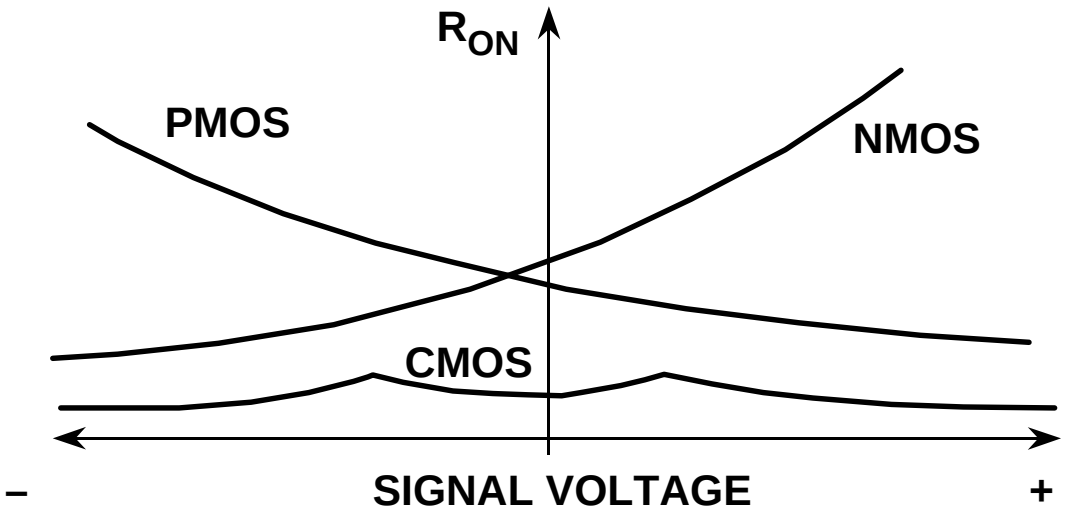
BASIC CMOS ANALOG SWITCH





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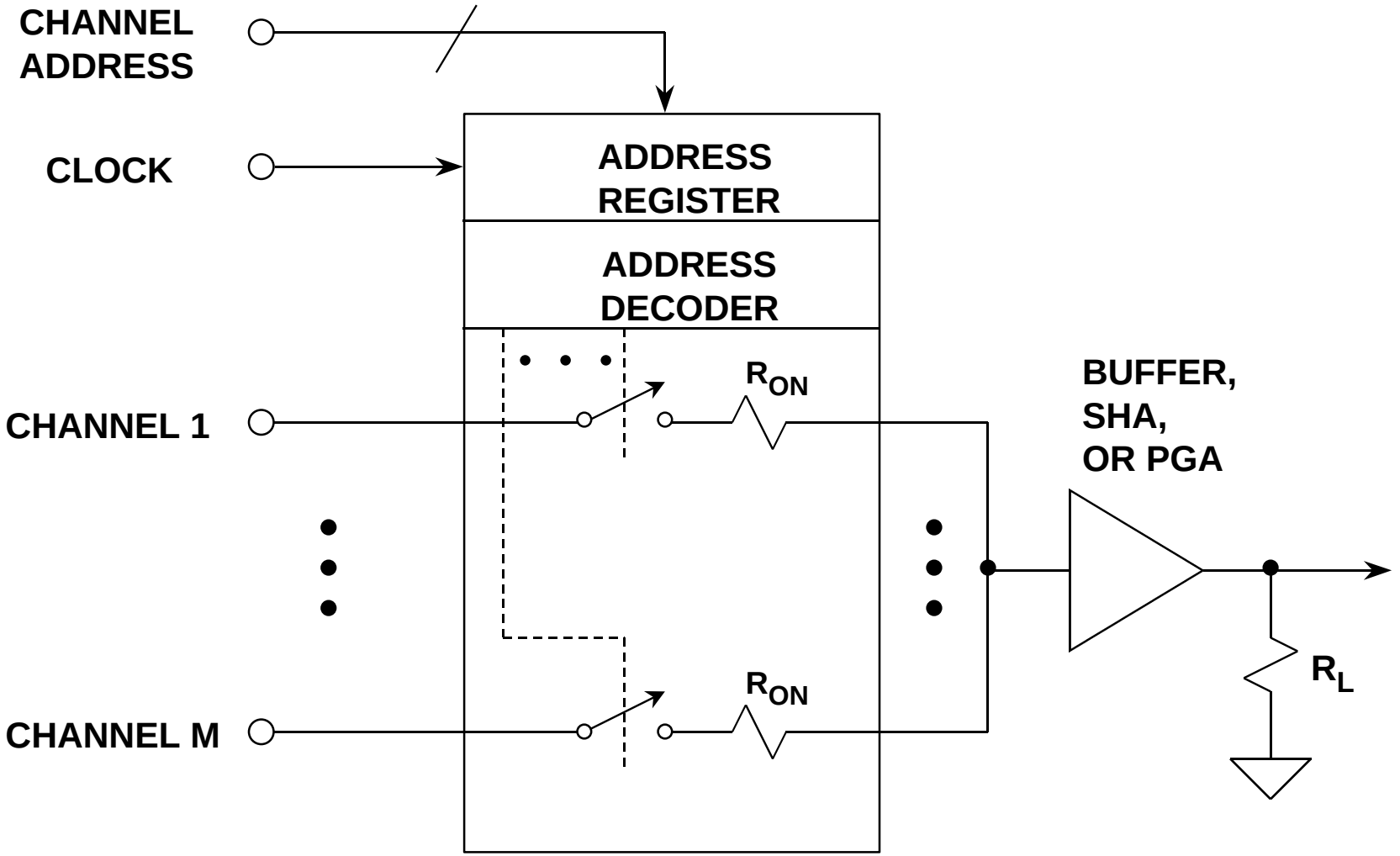
SIMPLIFIED DIAGRAM OF A TYPICAL ANALOG MULTIPLEXER



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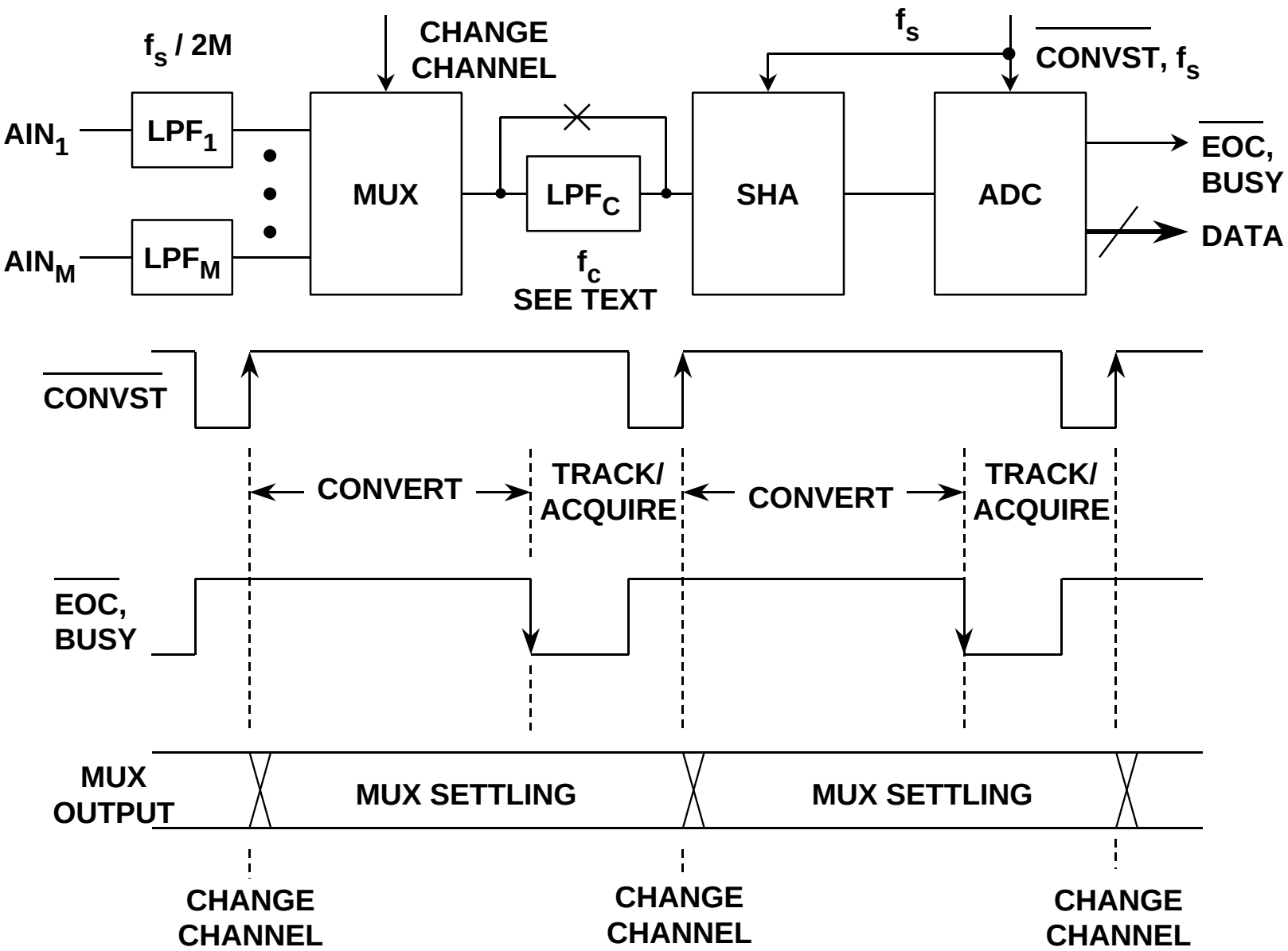
WHAT'S NEW IN DISCRETE SWITCHES / MUXES?

- **ADG508F, ADG509F, ADG527F: ±15V Specified**
  - **R_{ON} < 300Ω**
  - **Switching Time < 250ns**
  - **Fault Protection on Inputs and Outputs (–40V to + 55V)**

- **ADG451, ADG452, ADG453: ±15V, +12V, ±5V Specified**
  - **R_{ON} < 5Ω**
  - **Switching Time < 180ns**
  - **2kV ESD Protection**

- **ADG7XX-Family: Single-Supply, +1.8V to +5.5V**
  - **R_{ON} < 5Ω, R_{ON} Flatness < 2Ω**
  - **Switching Time < 20ns**

MULTIPLEXED SAR ADC FILTERING AND TIMING



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SINGLE-POLE FILTER SETTLING TIME TO REQUIRED ACCURACY

RESOLUTION # OF BITS	LSB (%FS)	# OF TIME CONSTANTS, n	f_c/f_s
6	1.563	4.16	0.67
8	0.391	5.55	0.89
10	0.0977	6.93	1.11
12	0.0244	8.32	1.32
14	0.0061	9.70	1.55
16	0.00153	11.09	1.77
18	0.00038	12.48	2.00
20	0.000095	13.86	2.22
22	0.000024	15.25	2.44

f_s = ADC Sampling Frequency
f_c = Cutoff Frequency of LPF_C

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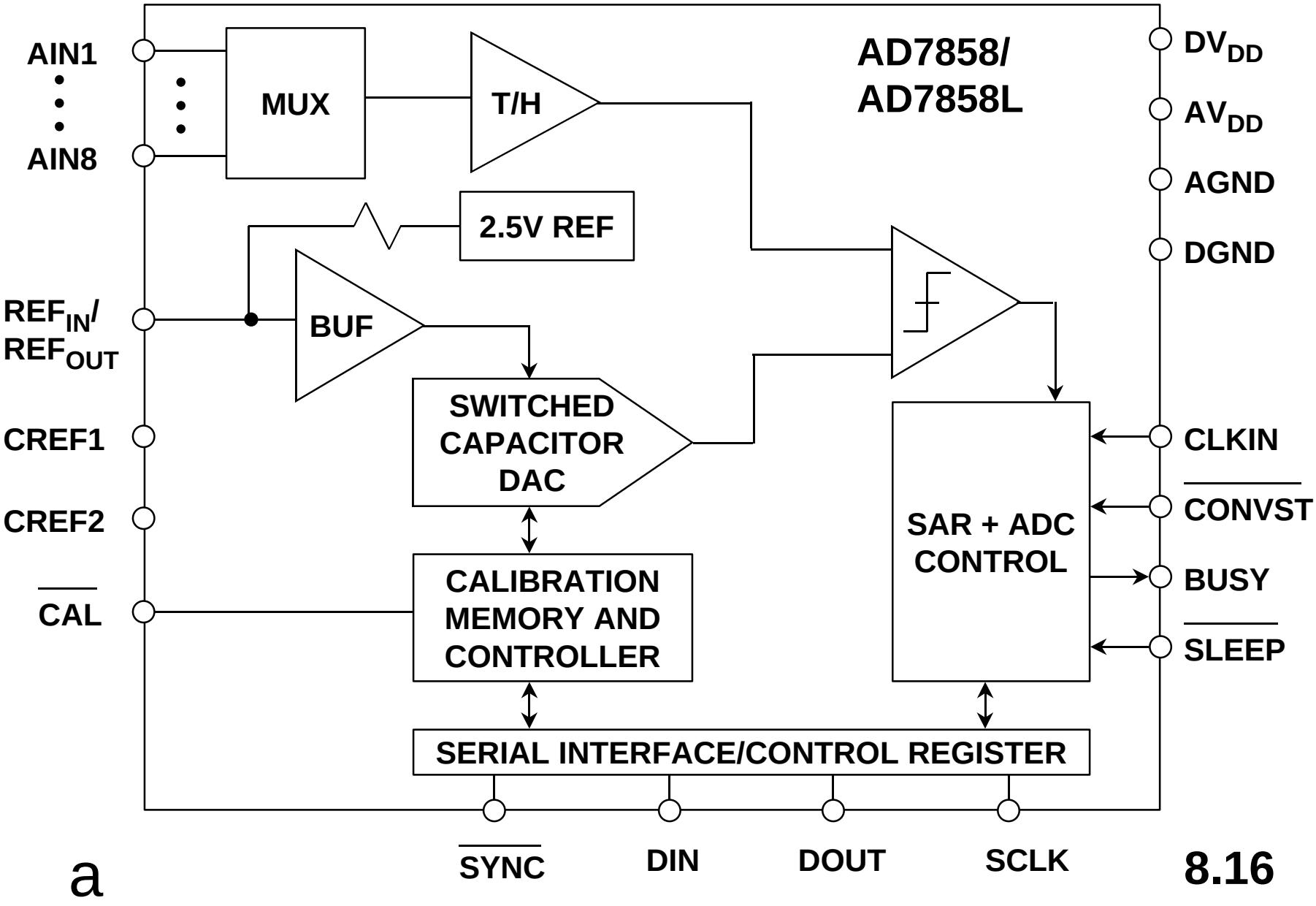
AD7858 12-BIT, 200kSPS 8-CHANNEL SINGLE-SUPPLY ADC



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AD7858 / AD7858L DATA ACQUISITION ADCs
KEY SPECIFICATIONS

- **12-Bit, 8Channel, 200kSPS (AD7858), 100kSPS (AD7858L)**
- **System and Self-Calibration with Autocalibration on Power-Up**
- **Automatic Power Down After Conversion (25µW)**
- **Low Power:**
  - **AD7858: 15mW (V_{DD} = +3V)**
  - **AD7858L: 5.5mW (V_{DD} = +3V)**
- **Flexible Serial Interface: 8051 / SPI / QSPI / µP Compatible**
- **24-Pin DIP, SOIC, SSOP Packages**
- **AD7859, AD7859L: Parallel Output Devices, Similar Specifications**

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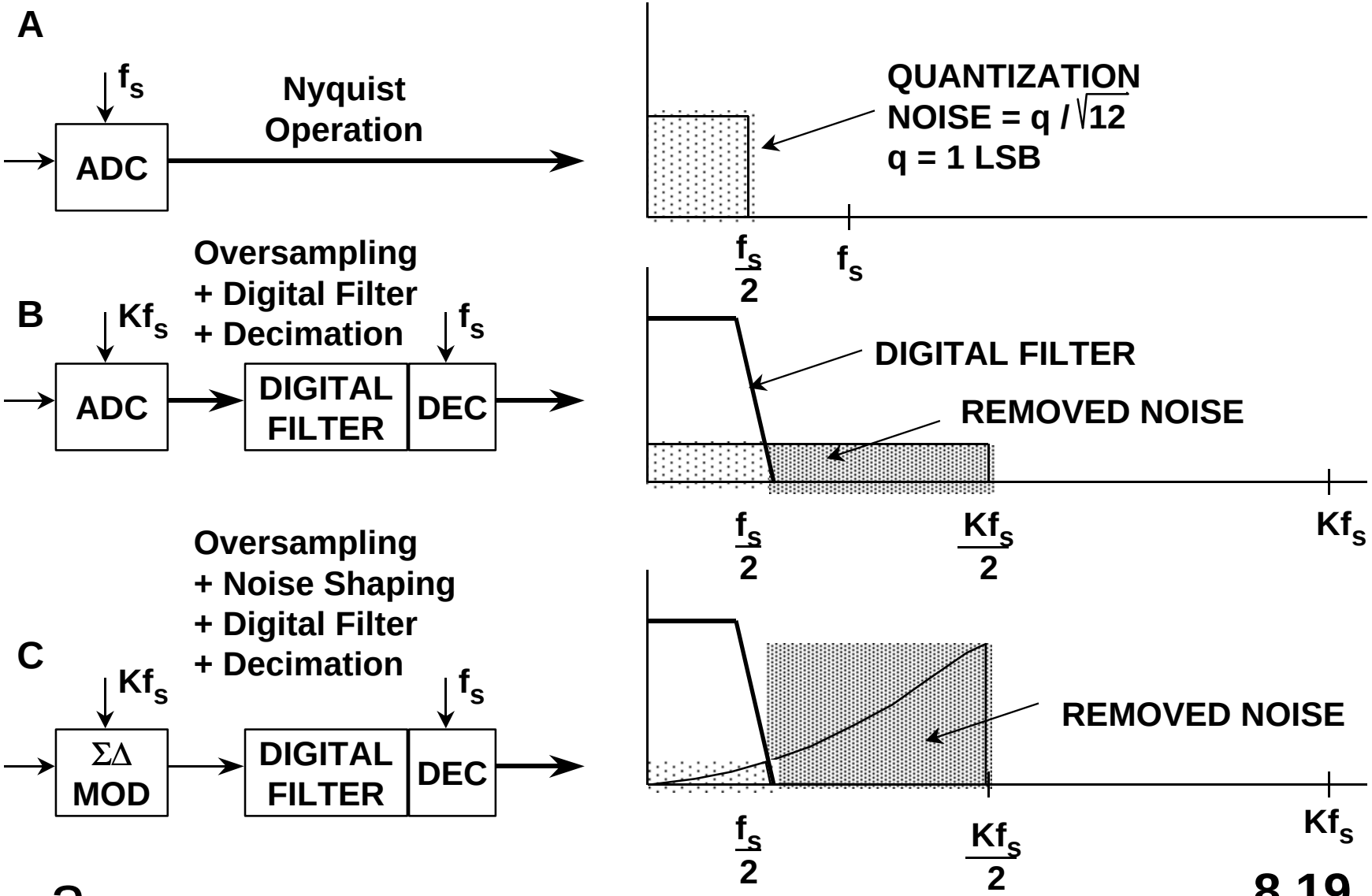
SIGMA-DELTA ADCs

- Low Cost, High Resolution (to 24-bits) Excellent DNL,
- Low Power, but Limited Bandwidth
- Key Concepts are Simple, but Math is Complex
  - Oversampling
  - Quantization Noise Shaping
  - Digital Filtering
  - Decimation
- Ideal for Sensor Signal Conditioning
  - High Resolution
  - Self, System, and Auto Calibration Modes

OVERSAMPLING, DIGITAL FILTERING, NOISE SHAPING, AND DECIMATION



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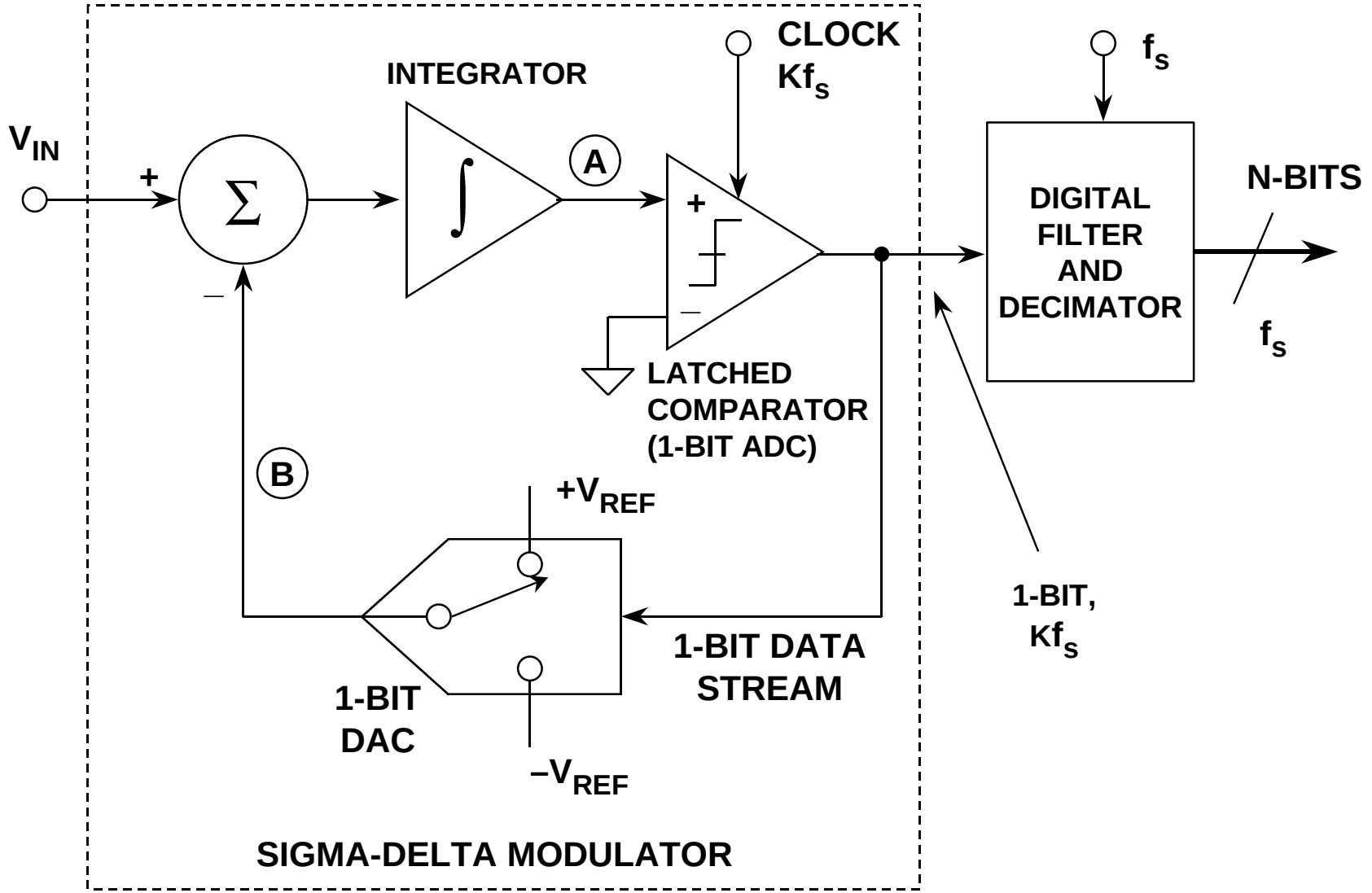
FIRST-ORDER SIGMA-DELTA ADC



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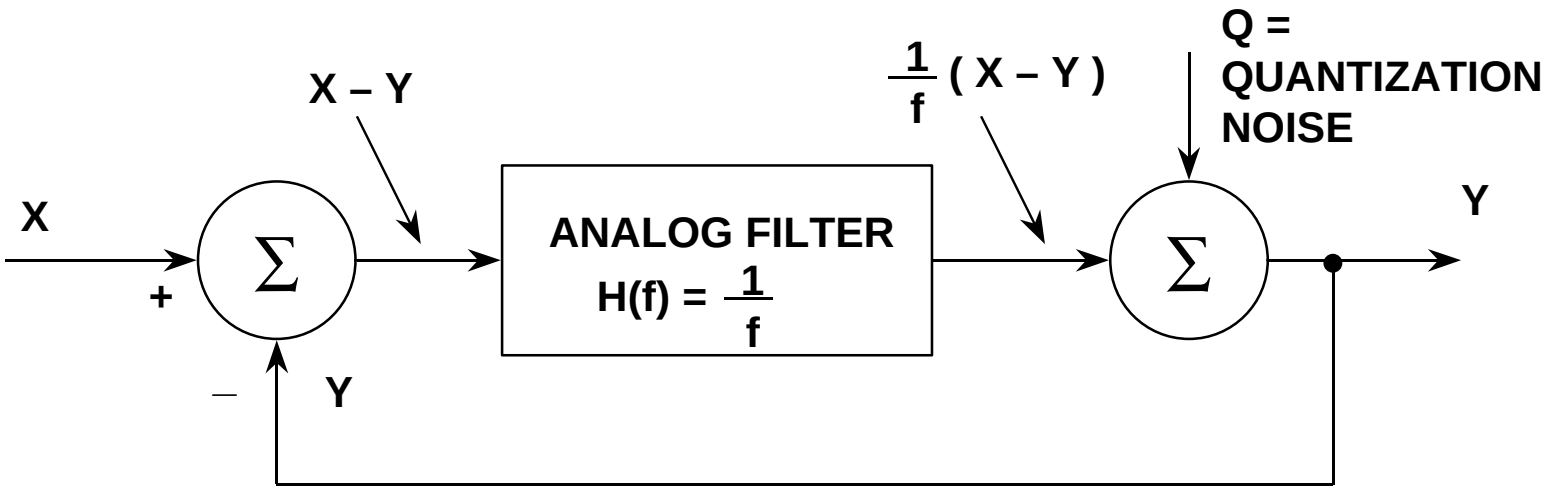
SIMPLIFIED FREQUENCY DOMAIN LINEARIZED MODEL OF A SIGMA-DELTA MODULATOR



$$Y = \frac{1}{f}(X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \frac{X}{f+1} + \frac{Q\,f}{f+1}$$

SIGNAL TERM **NOISE TERM**

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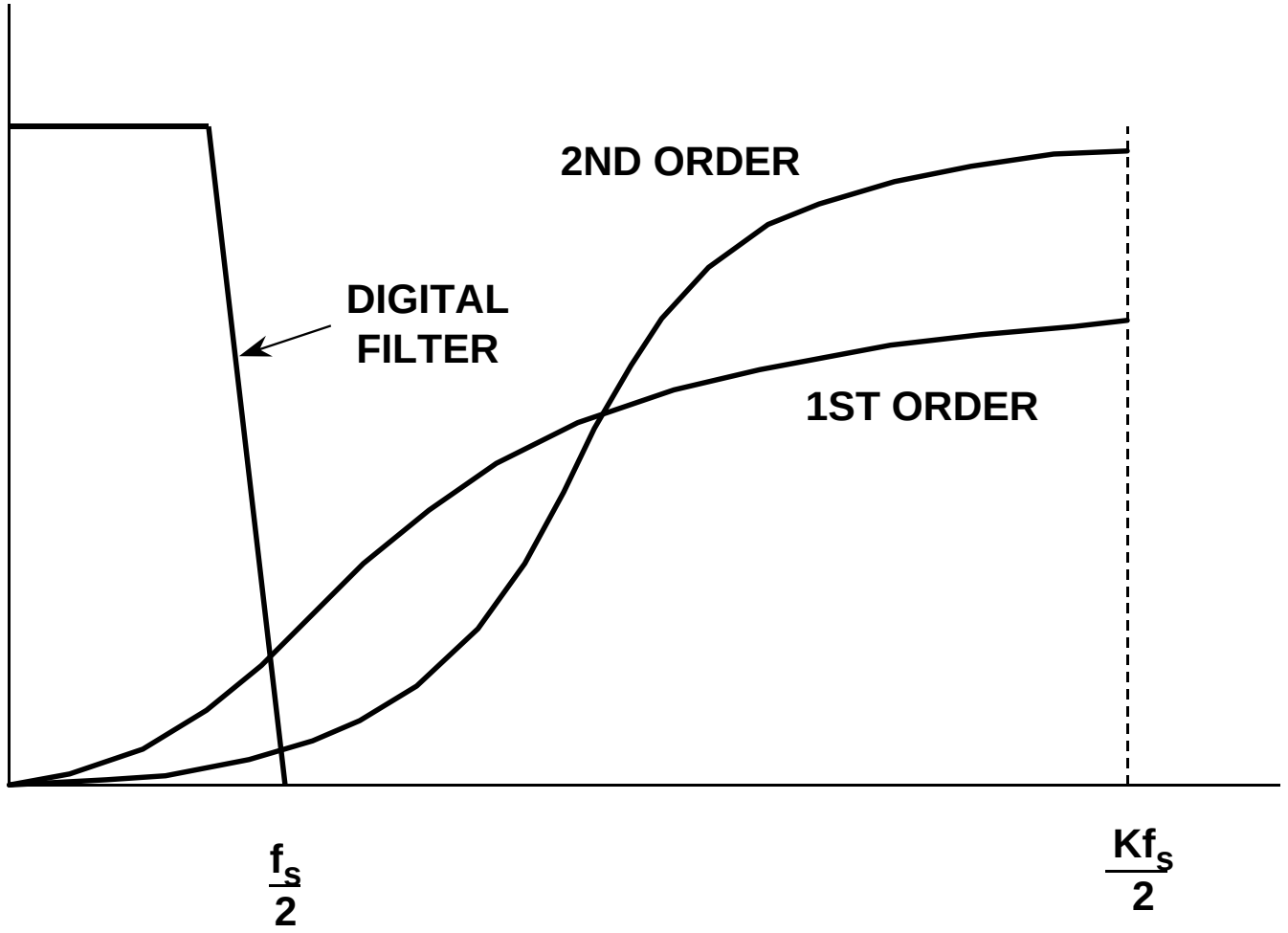
SIGMA-DELTA MODULATORS
SHAPE QUANTIZATION NOISE



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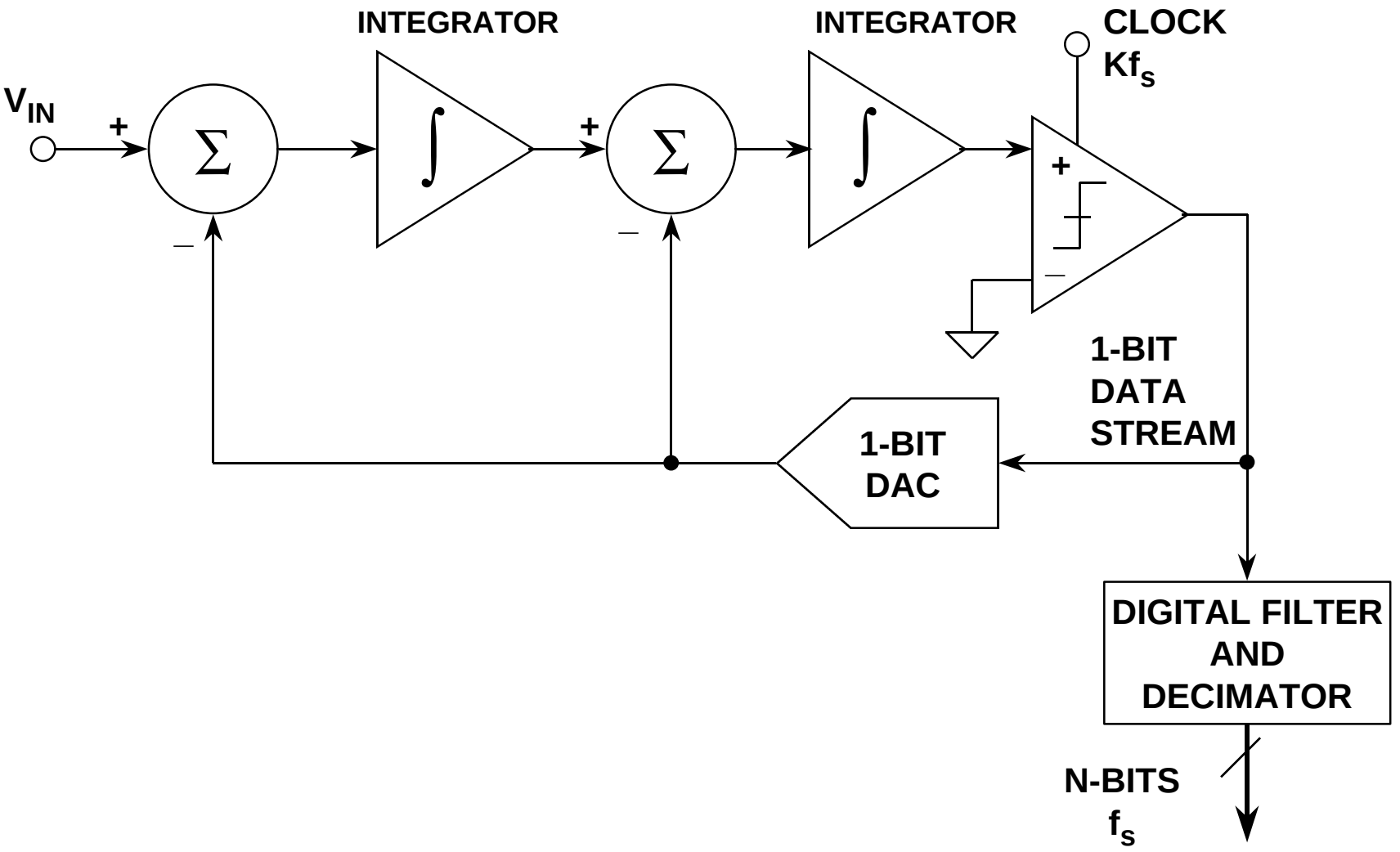
SECOND-ORDER SIGMA-DELTA ADC



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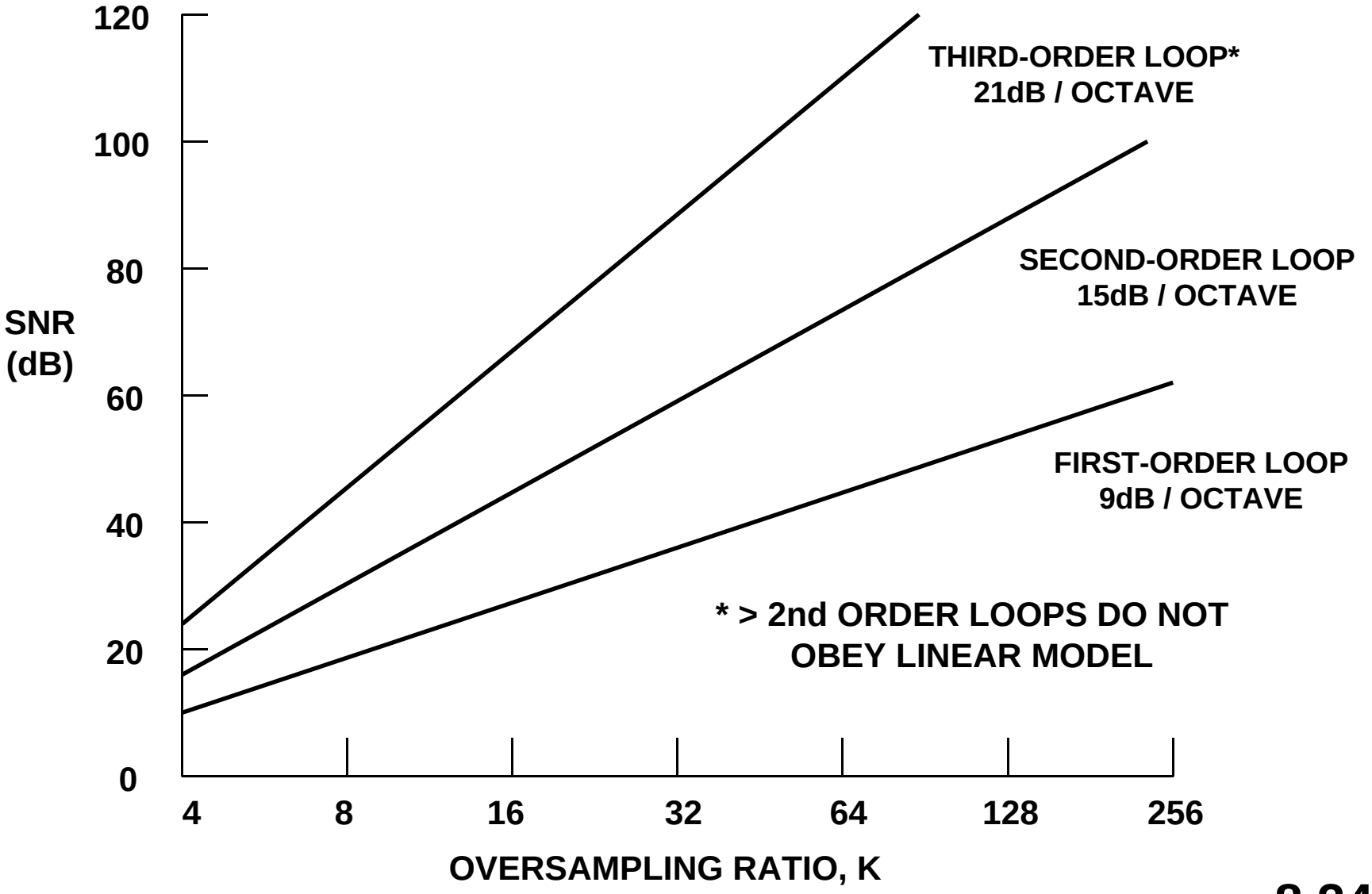
SNR VERSUS OVERSAMPLING RATIO FOR FIRST, SECOND, AND THIRD-ORDER LOOPS



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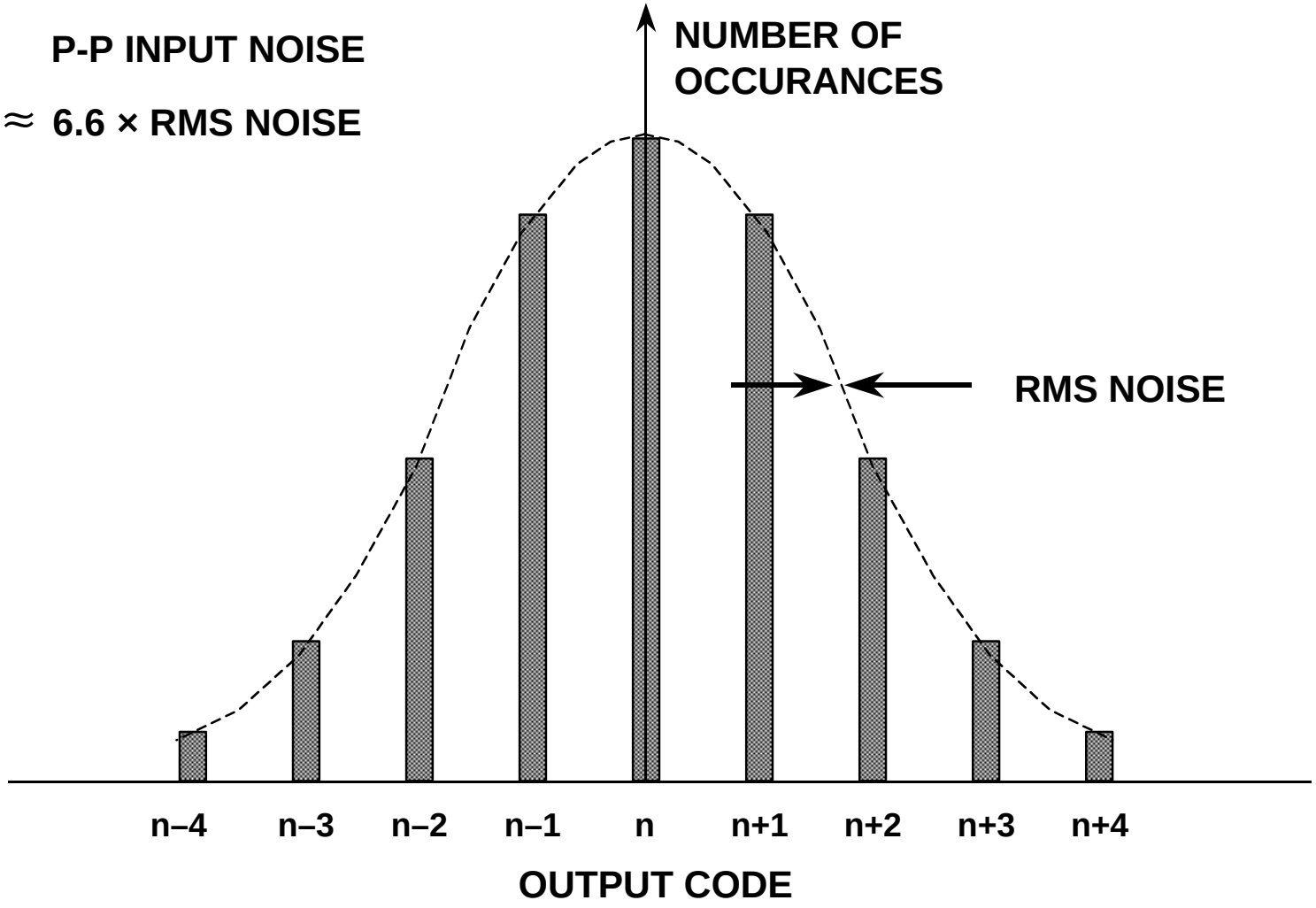
EFFECT OF INPUT-REFERRED NOISE ON ADC "GROUNDED INPUT" HISTOGRAM



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DEFINITION OF "NOISE-FREE" CODE RESOLUTION

- EFFECTIVE RESOLUTION = $\log_2 \left[\frac{\text{FULLSCALE RANGE}}{\text{RMS NOISE}} \right]$ BITS

- NOISE-FREE CODE RESOLUTION = $\log_2 \left[\frac{\text{FULLSCALE RANGE}}{\text{P-P NOISE}} \right]$ BITS

P-P NOISE = 6.6 × RMS NOISE

- NOISE-FREE CODE RESOLUTION = $\log_2 \left[\frac{\text{FULLSCALE RANGE}}{6.6 \times \text{RMS NOISE}} \right]$ BITS

= EFFECTIVE RESOLUTION – 2.72 BITS

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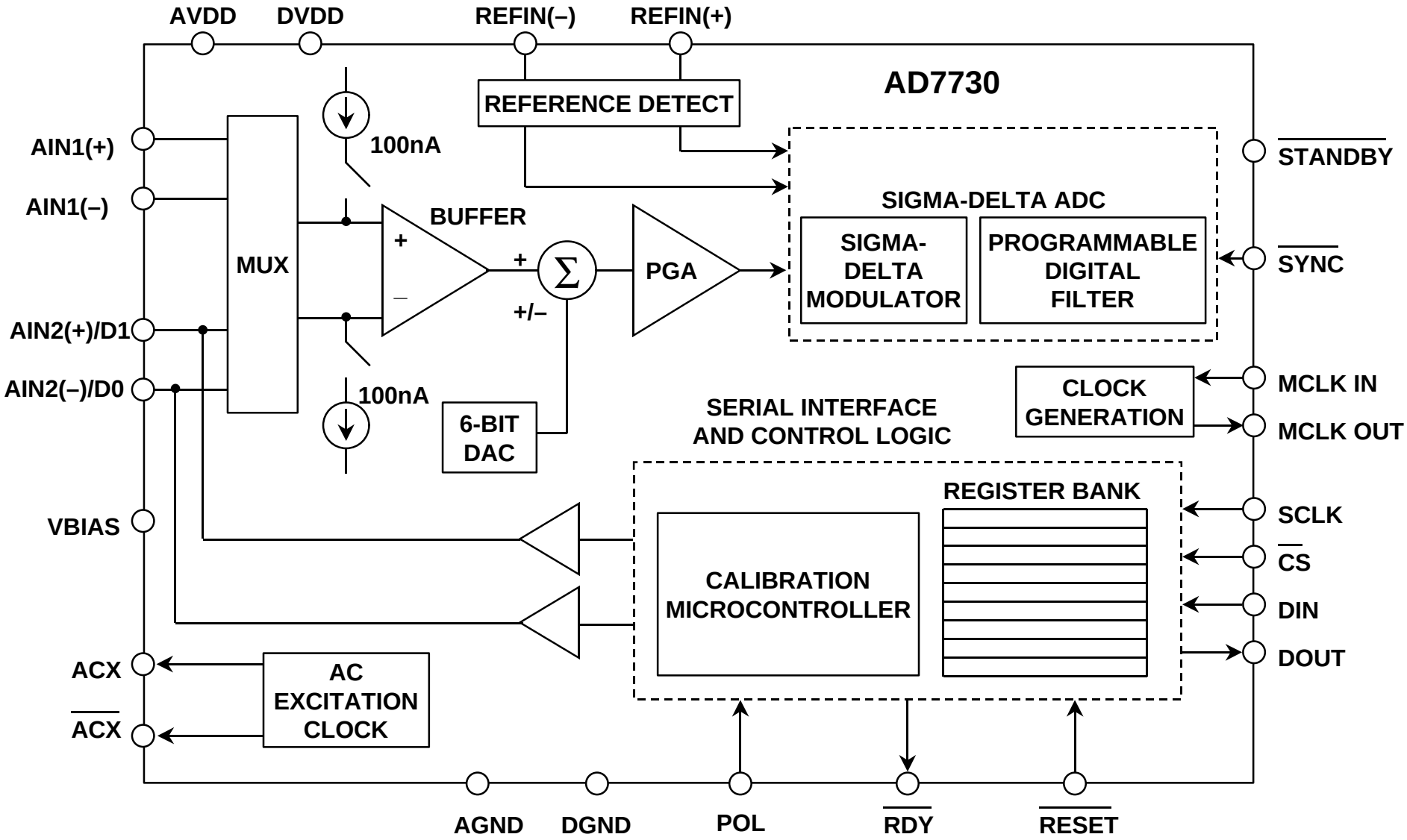
AD7730 SINGLE-SUPPLY BRIDGE ADC



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8.27

AD7730 KEY SPECIFICATIONS

- **Resolution of 80,000 Counts Peak-to-Peak (16.5-Bits) for ± 10mV Fullscale Range**
- **Chop Mode for Low Offset and Drift**
- **Offset Drift: 5nV/°C (Chop Mode Enabled)**
- **Gain Drift: 2ppm/°C**
- **Line Frequency Common Mode Rejection: > 150dB**
- **Two-Channel Programmable Gain Front End**
- **On-Chip DAC for Offset/TARE Removal**
- **FASTStep Mode**
- **AC Excitation Output Drive**
- **Internal and System Calibration Options**
- **Single +5V Supply**
- **Power Dissipation: 65mW, (125mW for 10mV FS Range)**
- **24-Lead SOIC and 24-Lead TSSOP Packages**

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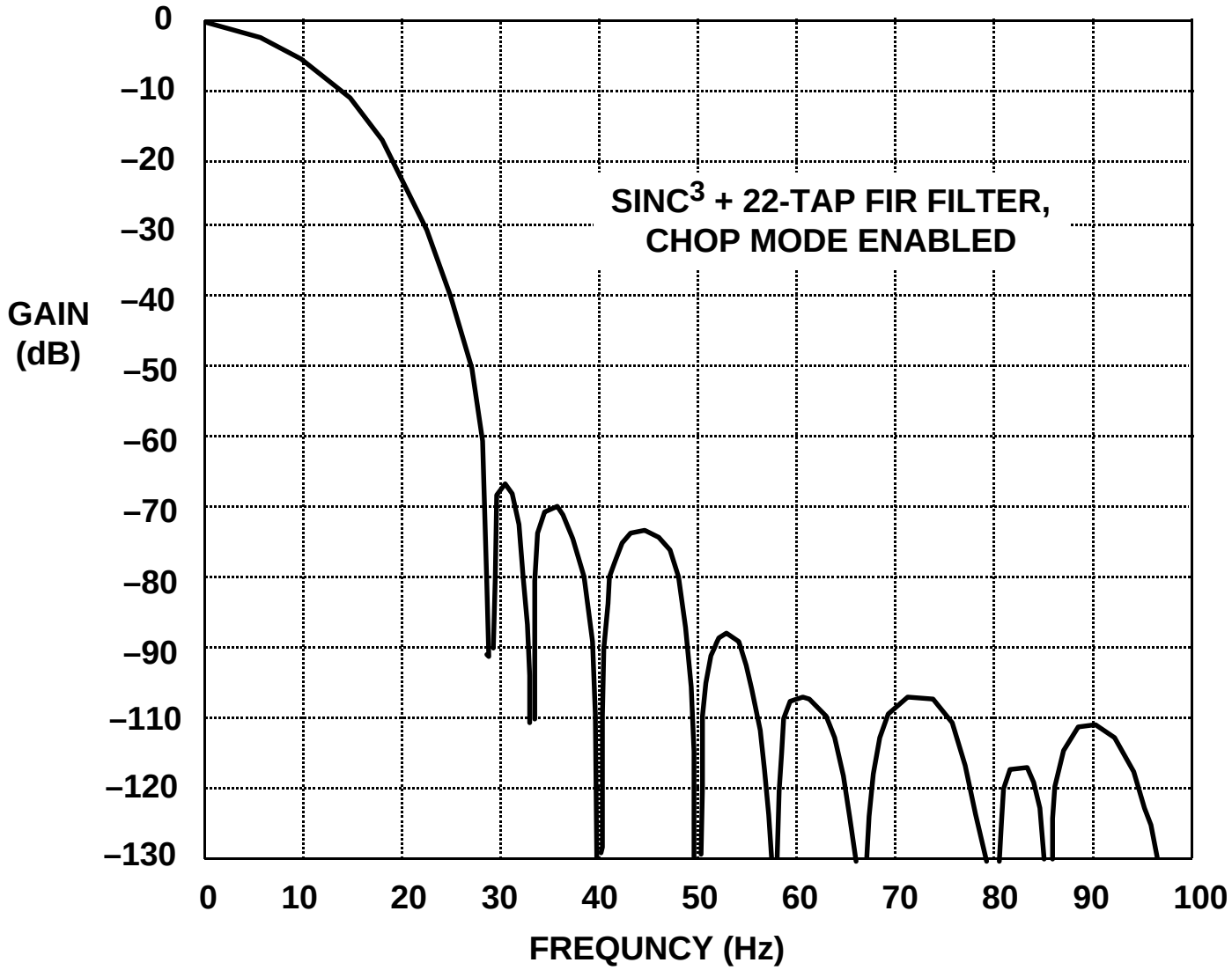
AD7730 DIGITAL FILTER FREQUENCY RESPONSE



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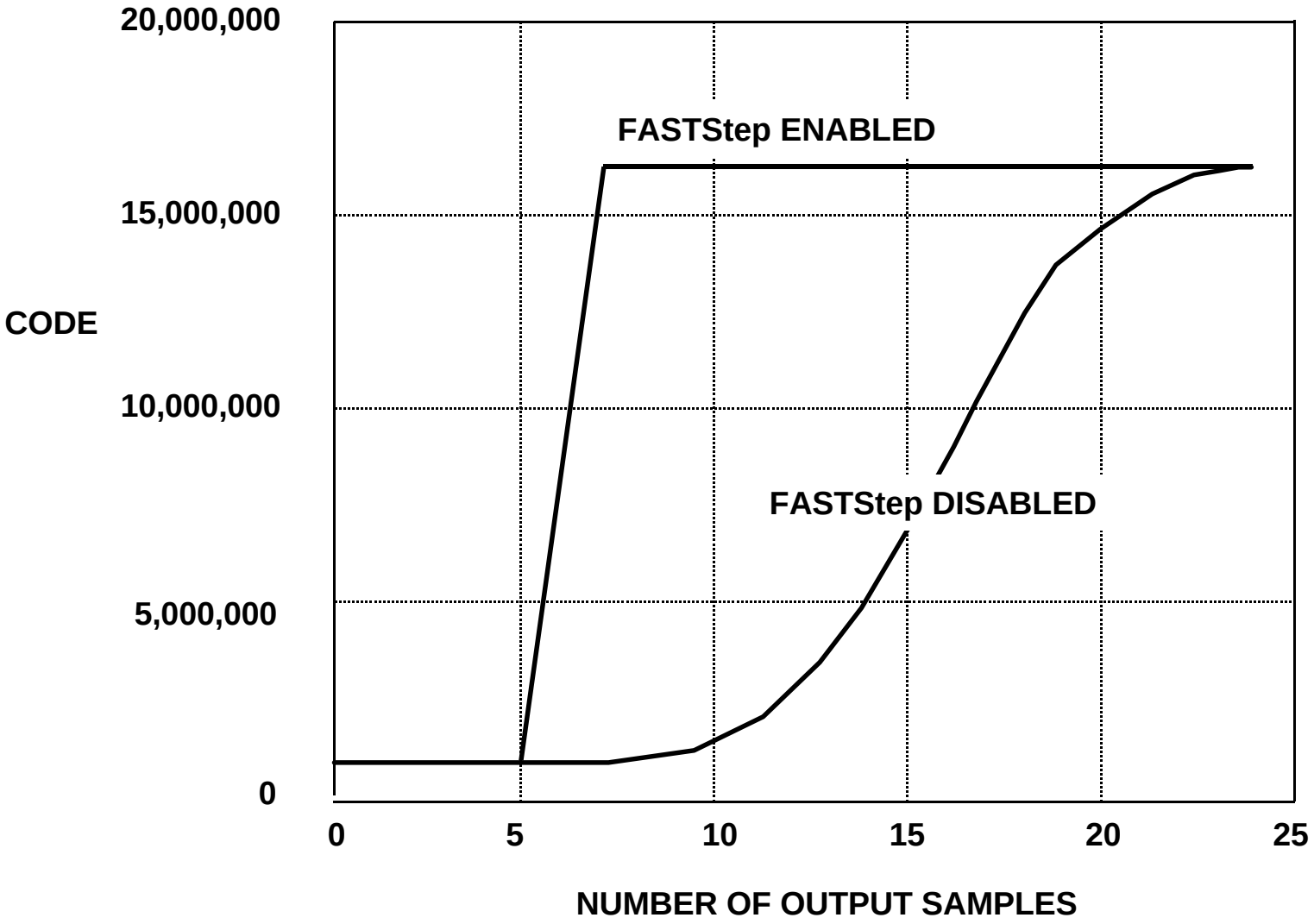
AD7730 DIGITAL FILTER SETTLING TIME SHOWING FASTStep™ MODE



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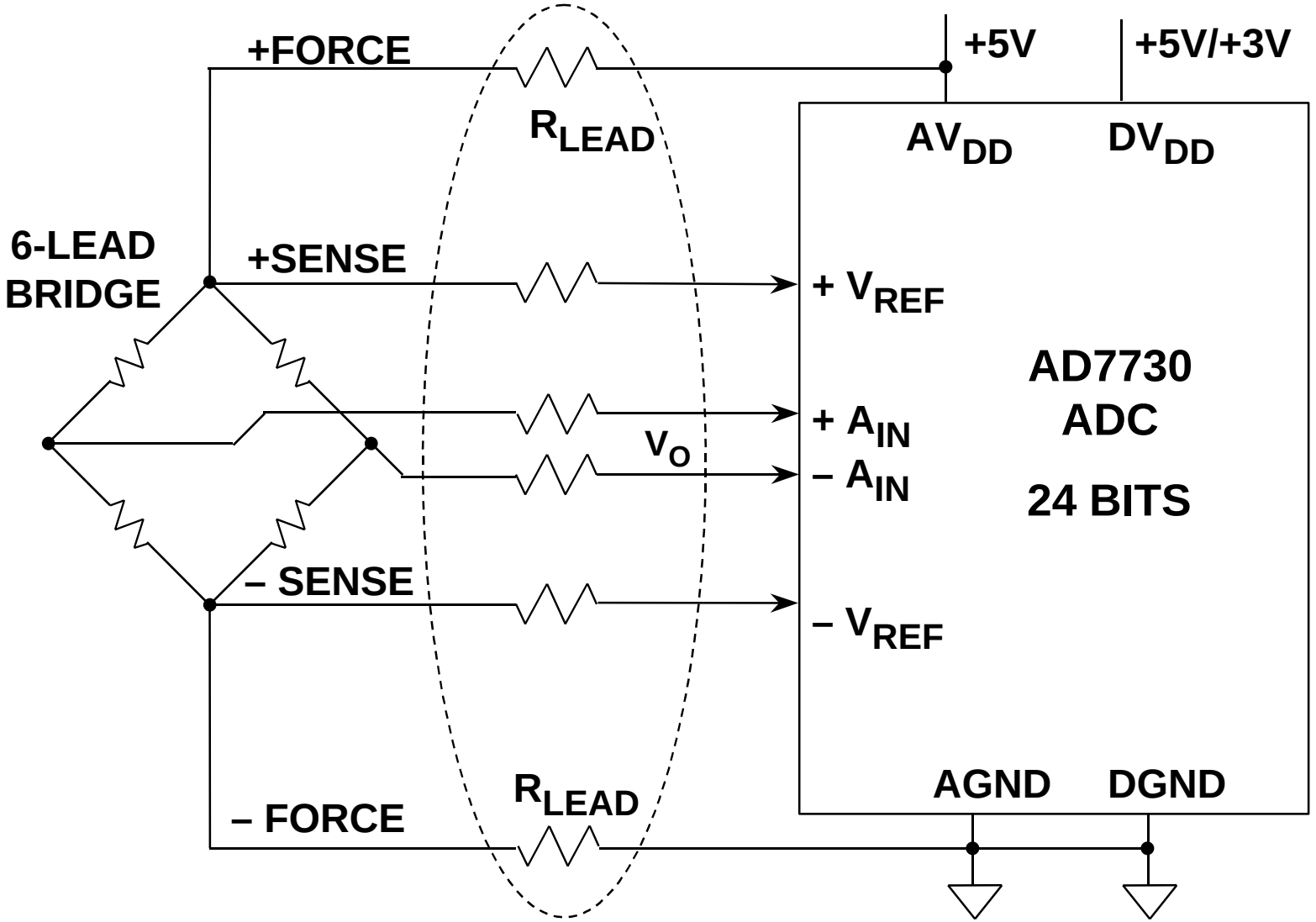
AD7730 SIGMA-DELTA ADC CALIBRATION OPTIONS

- **Internal Zero-ScaleCalibration**
  - **22 Output Cycles (CHP = 0)**
  - **24 Output Cycles (CHP = 1)**
- **Internal Full-Scale Calibration**
  - **44 Output Cycles (CHP = 0)**
  - **48 Output Cycles (CHP = 1)**
- **Calibration Programmed via the Mode Register**
- **Calibration Coefficients Stored in Calibration Registers**
- **External Microprocessor Can Read or Write to Calibration Coefficient Registers**

AD7730 BRIDGE APPLICATION (SIMPLIFIED SCHEMATIC)



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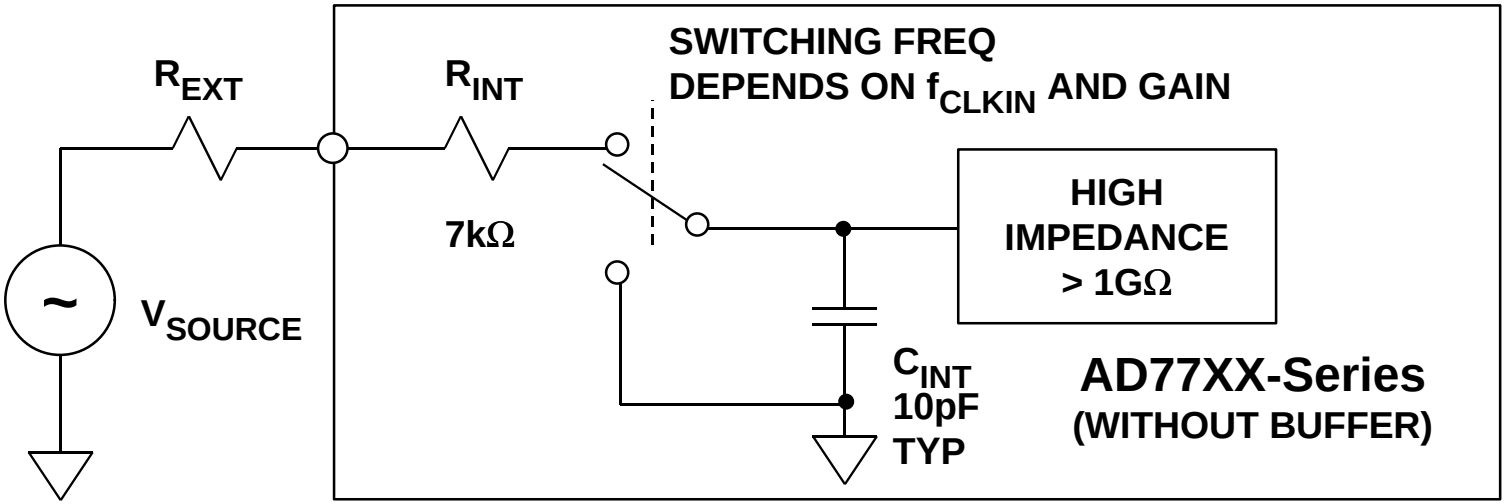
DRIVING UNBUFFERED AD77XX-SERIES ΣΔ ADC INPUTS



- R_{EXT} Increases C_{INT} Charge Time and May Result in Gain Error
- Charge Time Dependent on the Input Sampling Rate and Internal PGA Gain Setting
- Refer to Specific Data Sheet for Allowable Values of R_{EXT} to Maintain Desired Accuracy
- Some AD77XX-Series ADCs Have Internal Buffering Which Isolates Input from Switching Circuits

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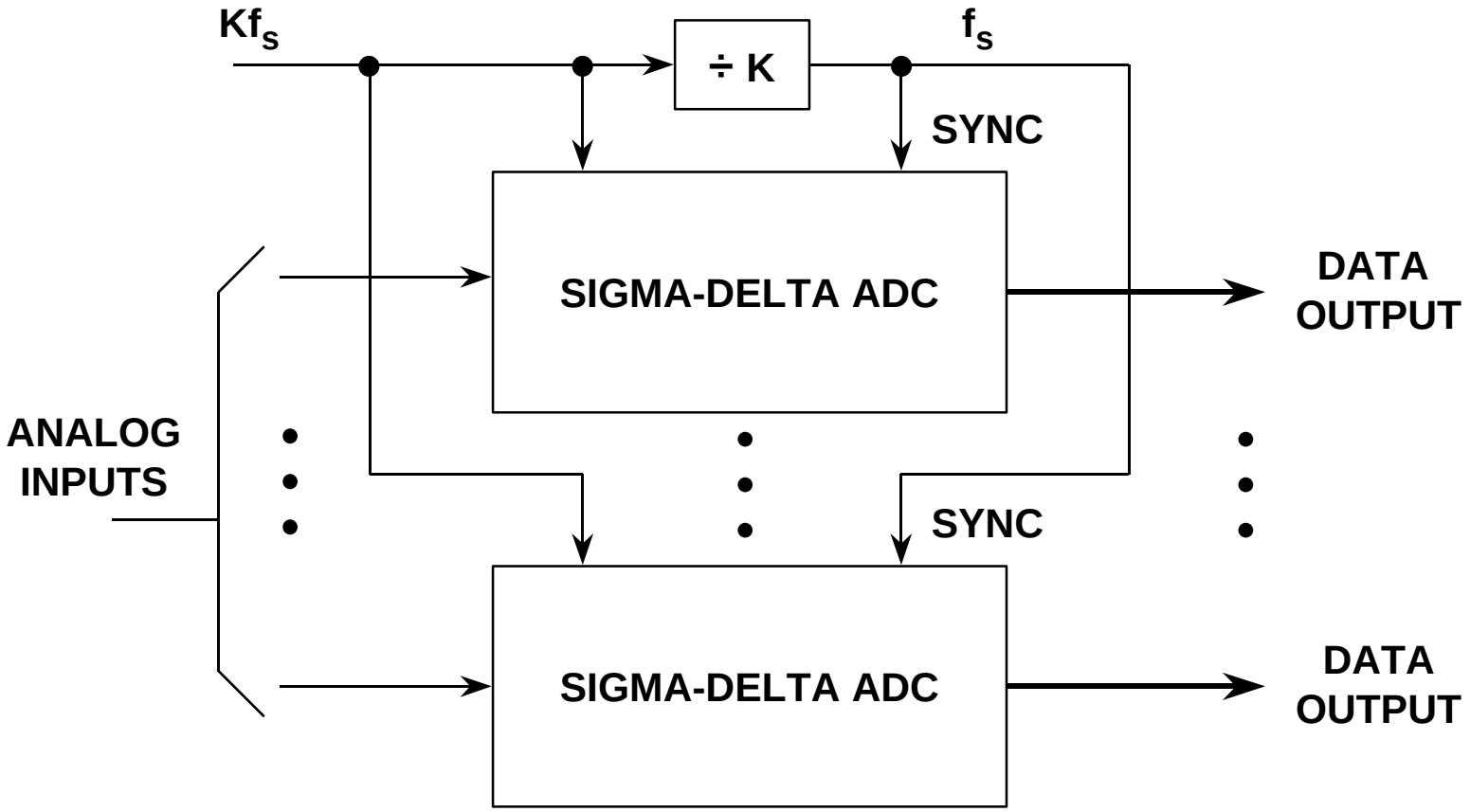
SYNCHRONIZING MULTIPLE SIGMA-DELTA ADCs IN SIMULTANEOUS SAMPLING APPLICATIONS



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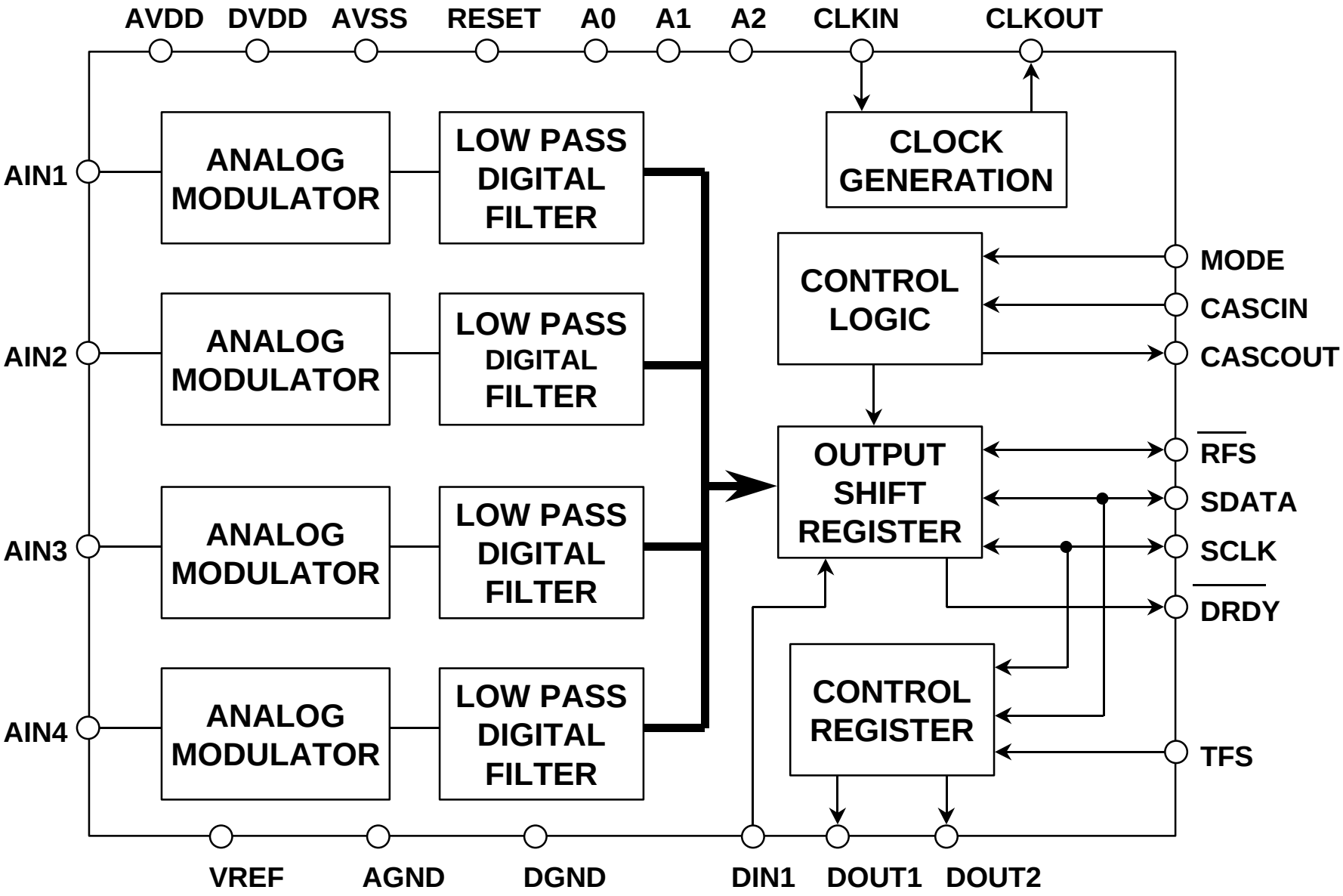
AD7716 MULTICHANNEL SIGMA-DELTA ADC



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AD7716 KEY SPECIFICATIONS

- **Up to 22-Bit Resolution, 4 Input Channels**
- **Sigma-Delta Architecture, 570kSPS Oversampling Rate**
- **On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz**
- **Serial Input / Output Interface**
- **±5V Power Supply Operation**
- **50mW Power Dissipation**

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BASICS OF POWER MEASUREMENTS

- $v(t) = V \times \cos(\omega t)$ (Instantaneous Voltage)
- $i(t) = I \times \cos(\omega t)$ (Instantaneous Current)
- $p(t) = V \times I \cos^2(\omega t)$ (Instantaneous Power)
- $p(t) = \frac{V \times I}{2} \left[1 + \cos(2\omega t)\right]$

Average Value of p(t) = Instantaneous *Real Power*

Includes Effects of Power Factor and Waveform Distortion

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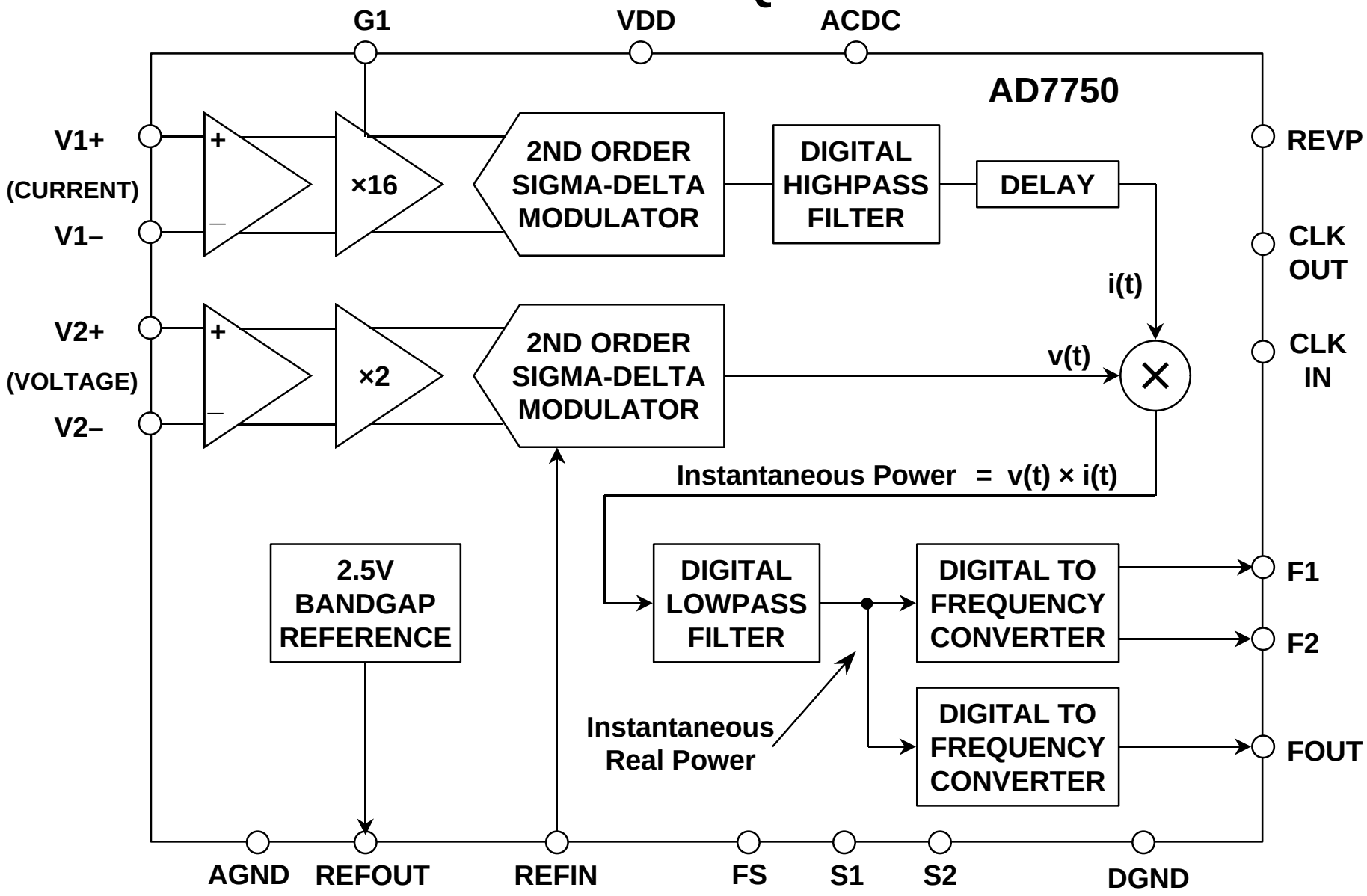
AD7750 PRODUCT-TO-FREQUENCY CONVERTER



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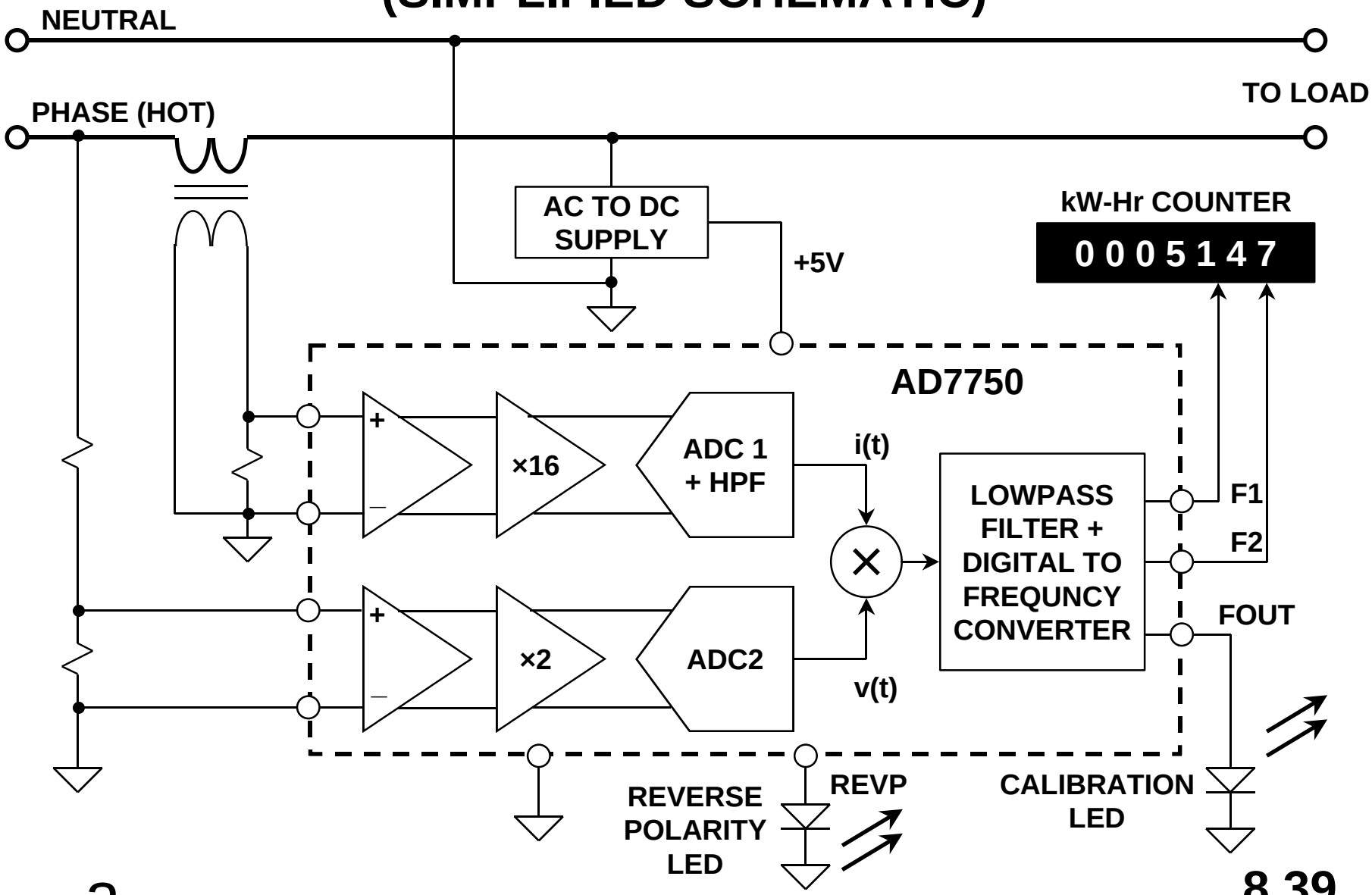
AD7750 SINGLE PHASE POWER METER APPLICATION (SIMPLIFIED SCHEMATIC)



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