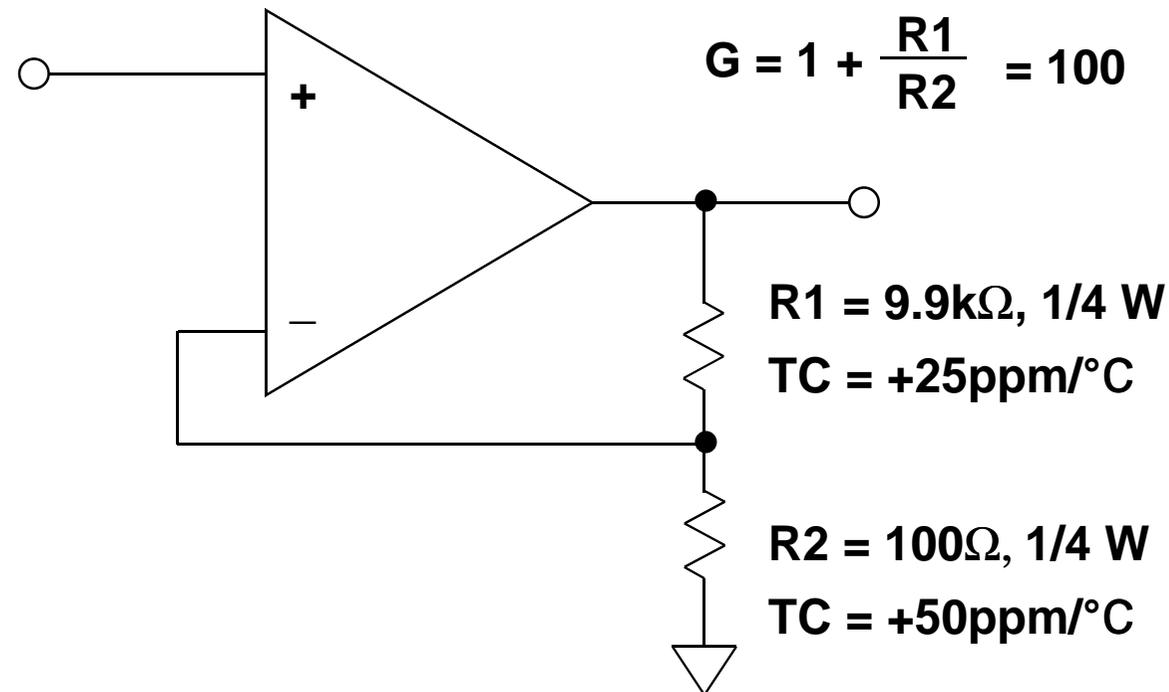


# **PRACTICAL DESIGN TECHNIQUES FOR SENSOR SIGNAL CONDITIONING**

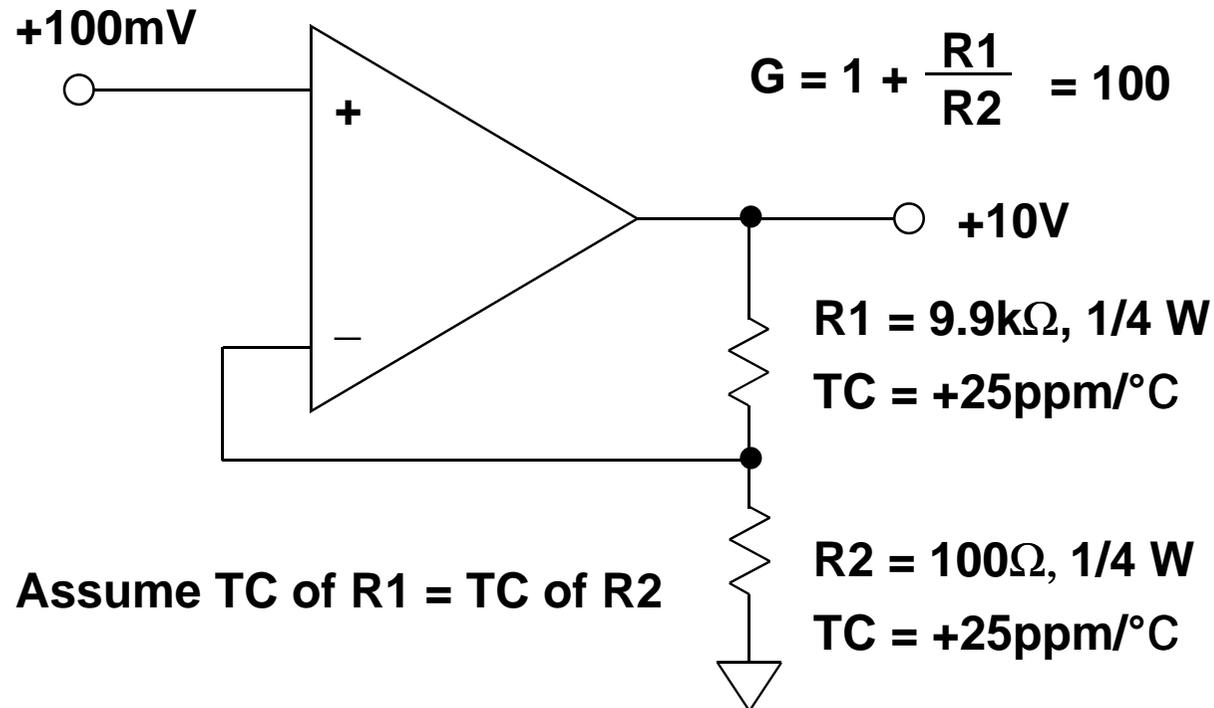
- 1 Introduction**
- 2 Bridge Circuits**
- 3 Amplifiers for Signal Conditioning**
- 4 Strain, Force, Pressure, and Flow Measurements**
- 5 High Impedance Sensors**
- 6 Position and Motion Sensors**
- 7 Temperature Sensors**
- 8 ADCs for Signal Conditioning**
- 9 Smart Sensors**
- 10 Hardware Design Techniques**

# RESISTOR TEMPERATURE COEFFICIENT MISMATCHES CAUSE GAIN VARIATION WITH TEMPERATURE



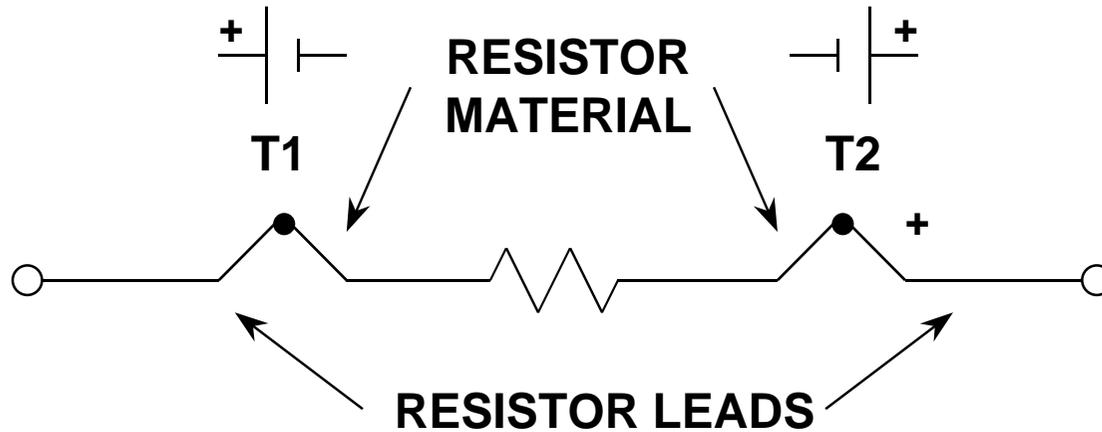
- Temperature change of  $10^\circ\text{C}$  causes gain change of 250ppm
- This is 1LSB in a 12-bit system and a disaster in a 16-bit system

# RESISTOR SELF-HEATING EVEN IN MATCHED RESISTORS CAN CAUSE GAIN VARIATION WITH INPUT LEVEL



- R1, R2 Thermal Resistance =  $125^{\circ}C / W$
- Temperature of R1 will rise by  $1.24^{\circ}C$ ,  $P_D = 9.9mW$
- Temperature rise of R2 is negligible,  $P_D = 0.1mW$
- Gain is altered by 31ppm, or 1/2 LSB @ 14-bits

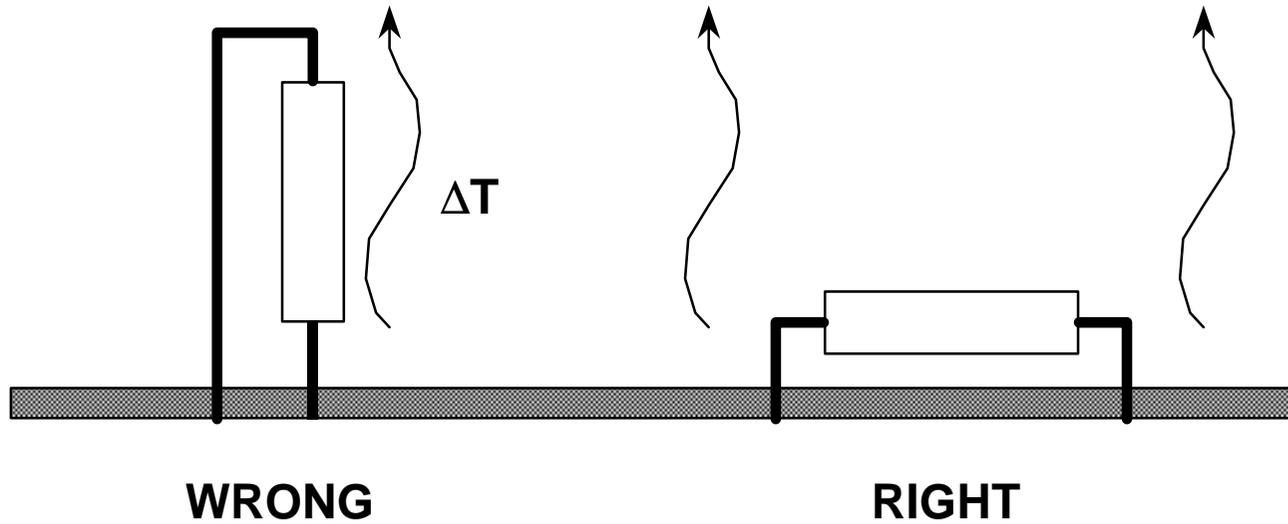
# RESISTORS CONTAIN THERMOCOUPLES



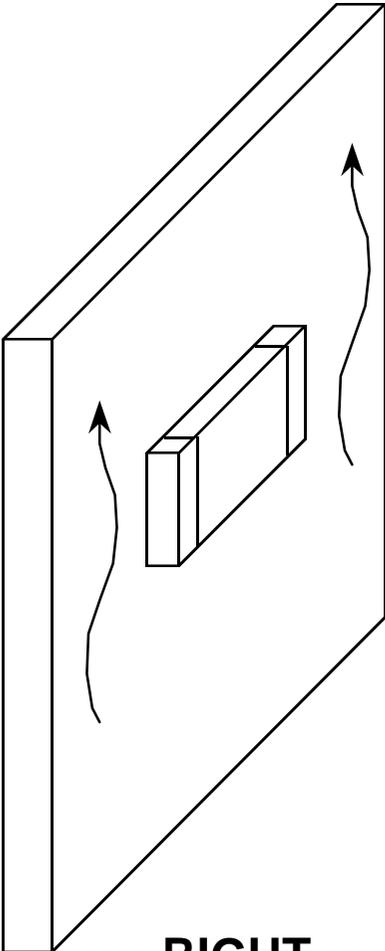
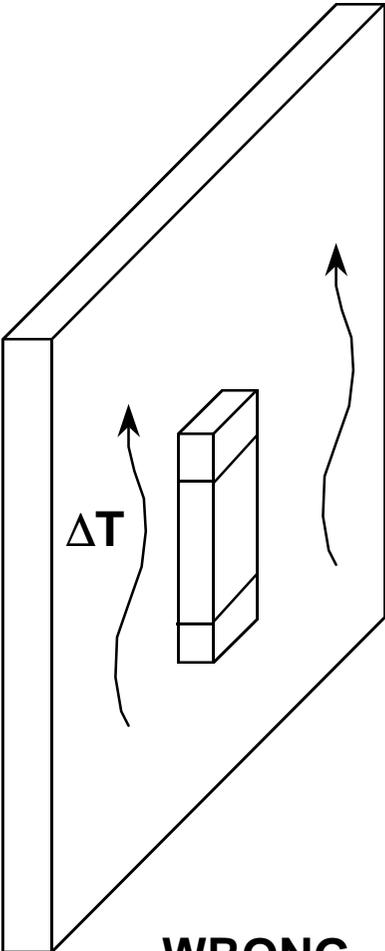
## TYPICAL RESISTOR THERMOCOUPLE EMFs

- CARBON COMPOSITION  $\approx 400 \mu\text{V}/^\circ\text{C}$
- METAL FILM  $\approx 20 \mu\text{V}/^\circ\text{C}$
- EVENOHM OR MANGANIN WIREWOUND  $\approx 2 \mu\text{V}/^\circ\text{C}$
- RCD Components HP-Series  $\approx 0.05 \mu\text{V}/^\circ\text{C}$

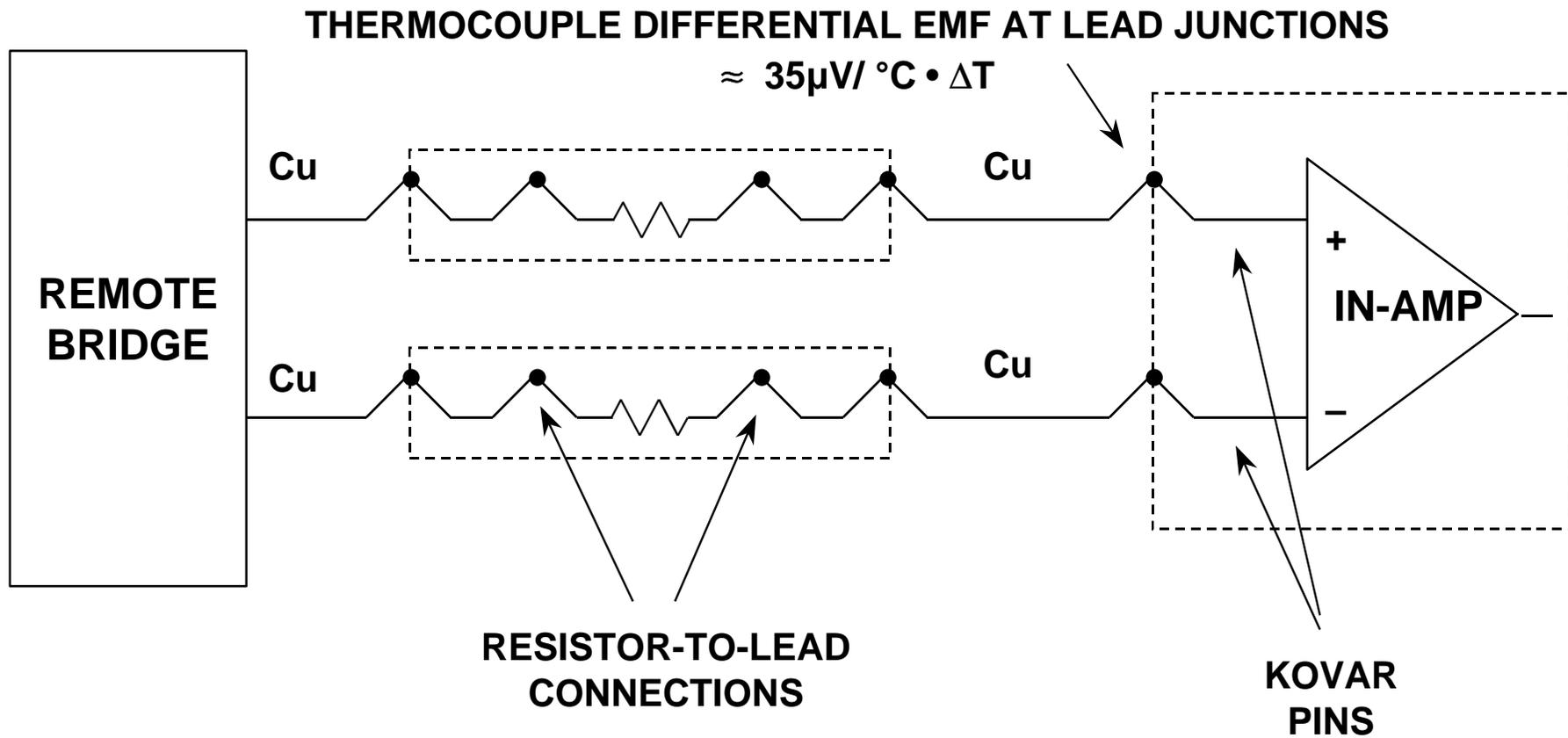
# AVOIDING THERMAL GRADIENTS MINIMIZES THERMOCOUPLE ERROR VOLTAGES



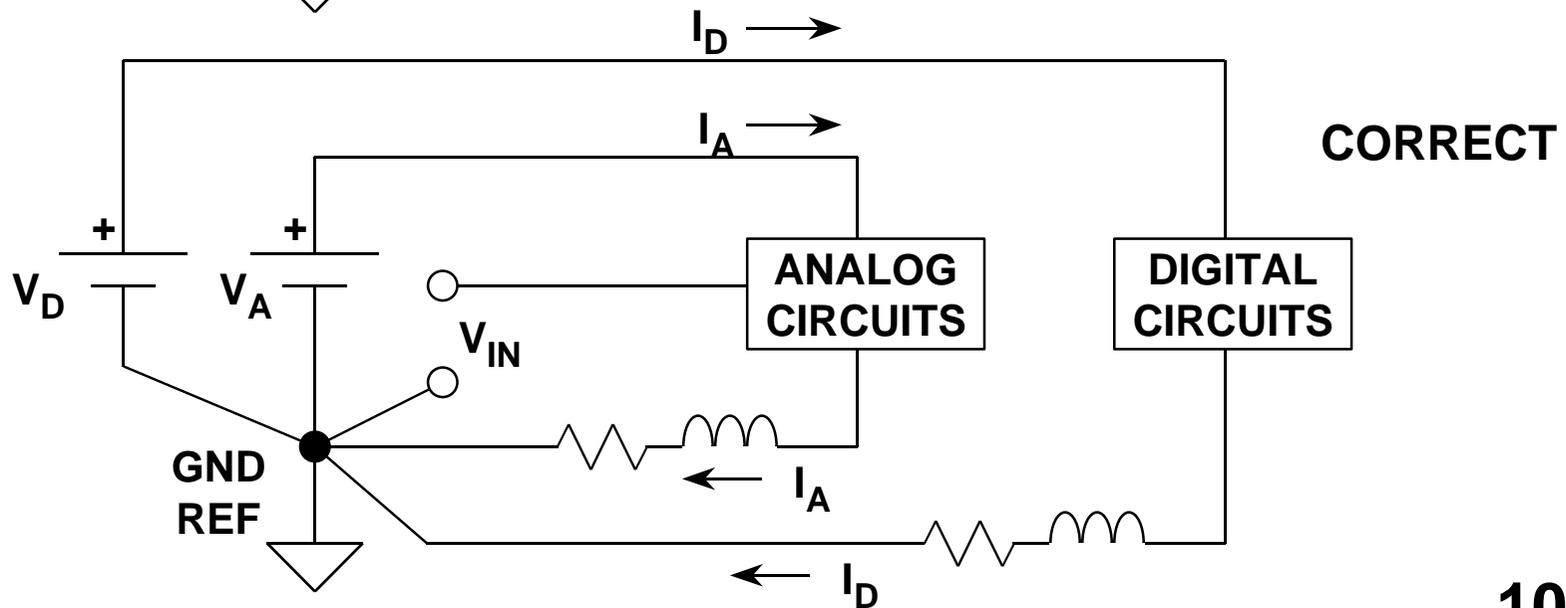
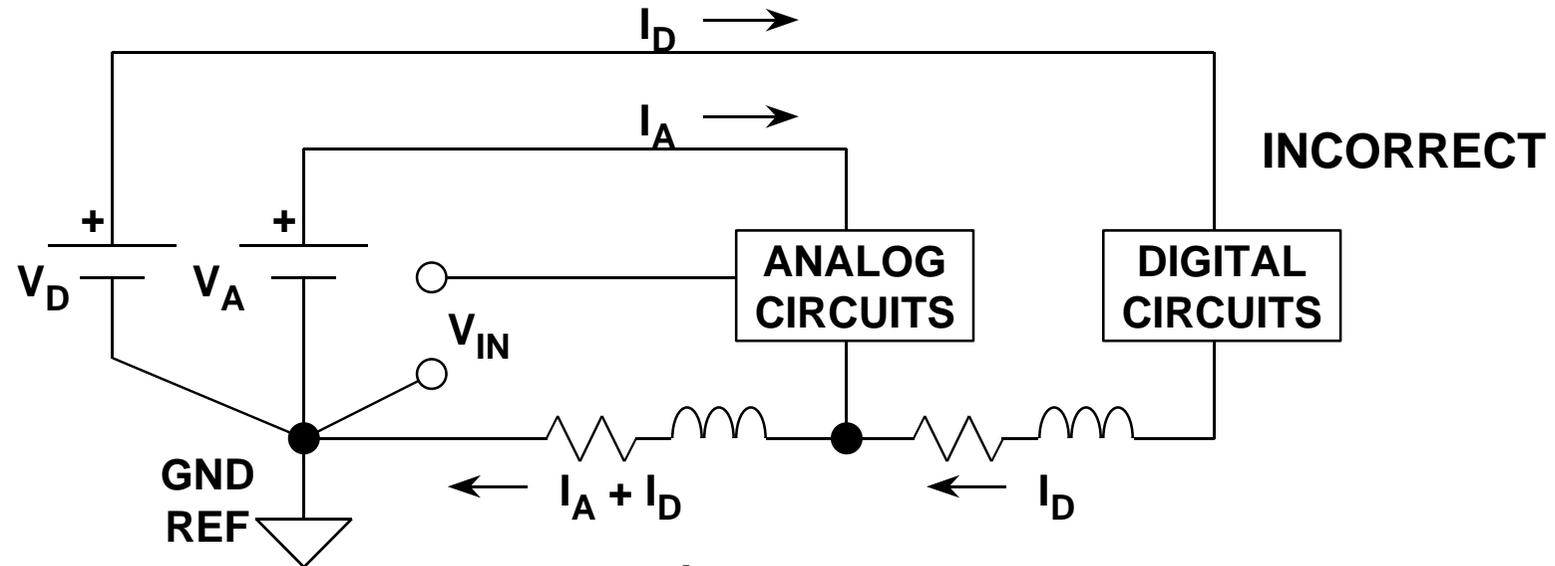
# PROPER ORIENTATION OF SURFACE MOUNT RESISTORS MINIMIZES THERMOCOUPLE ERROR VOLTAGE



# PARASITIC THERMOCOUPLES IN SIMPLE CIRCUIT



# DIGITAL CURRENTS FLOWING IN ANALOG RETURN PATH CREATE ERROR VOLTAGES



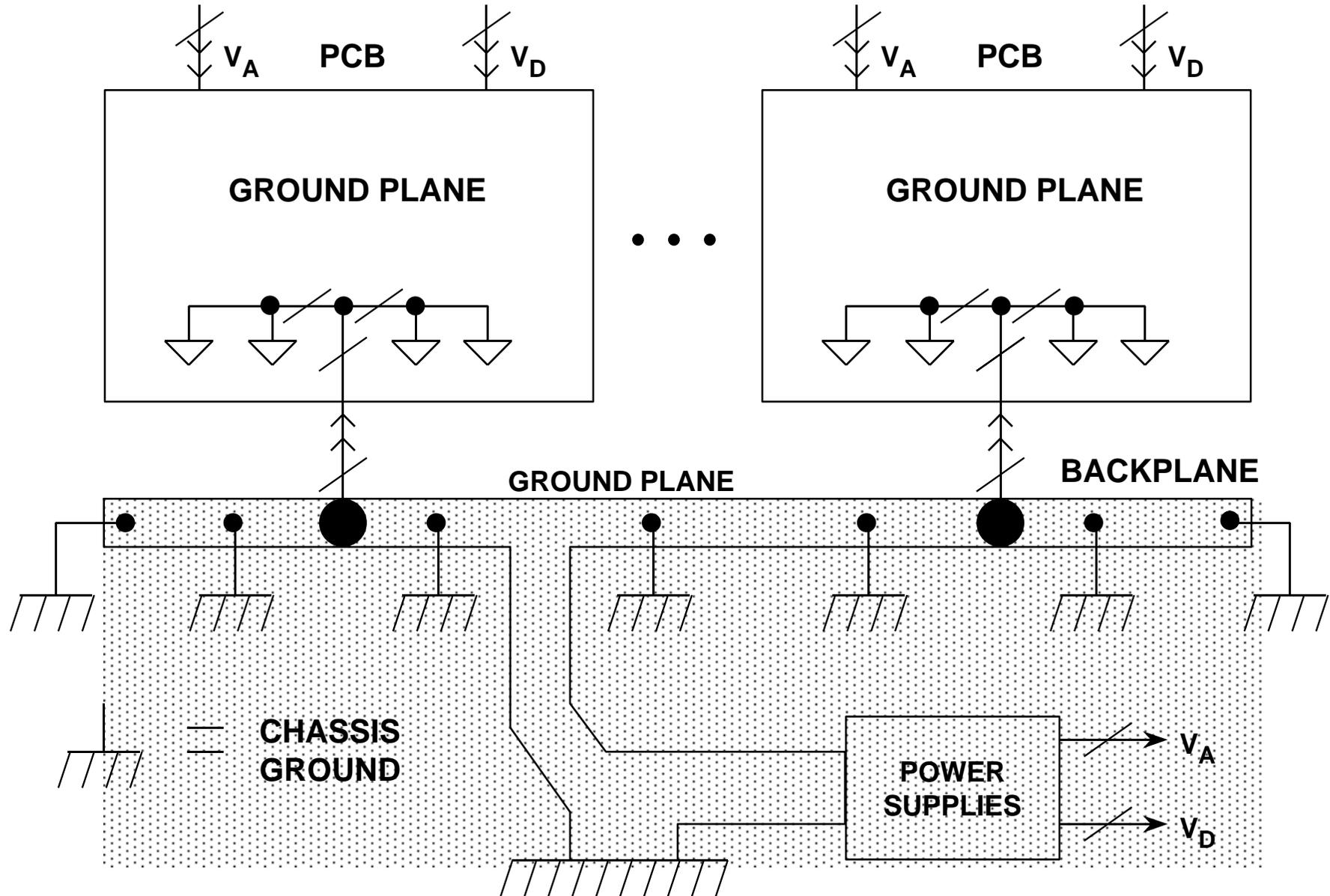
a

10.7

# **GROUND PLANES ARE MANDATORY!**

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
  - ◆ **Avoid High-Density Interconnection Crossovers and Feedthroughs Which Reduce Ground Plane Area**
  - ◆ **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards**
  - ◆ **Dedicate at Least One Layer for the Ground Plane**
  - ◆ **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

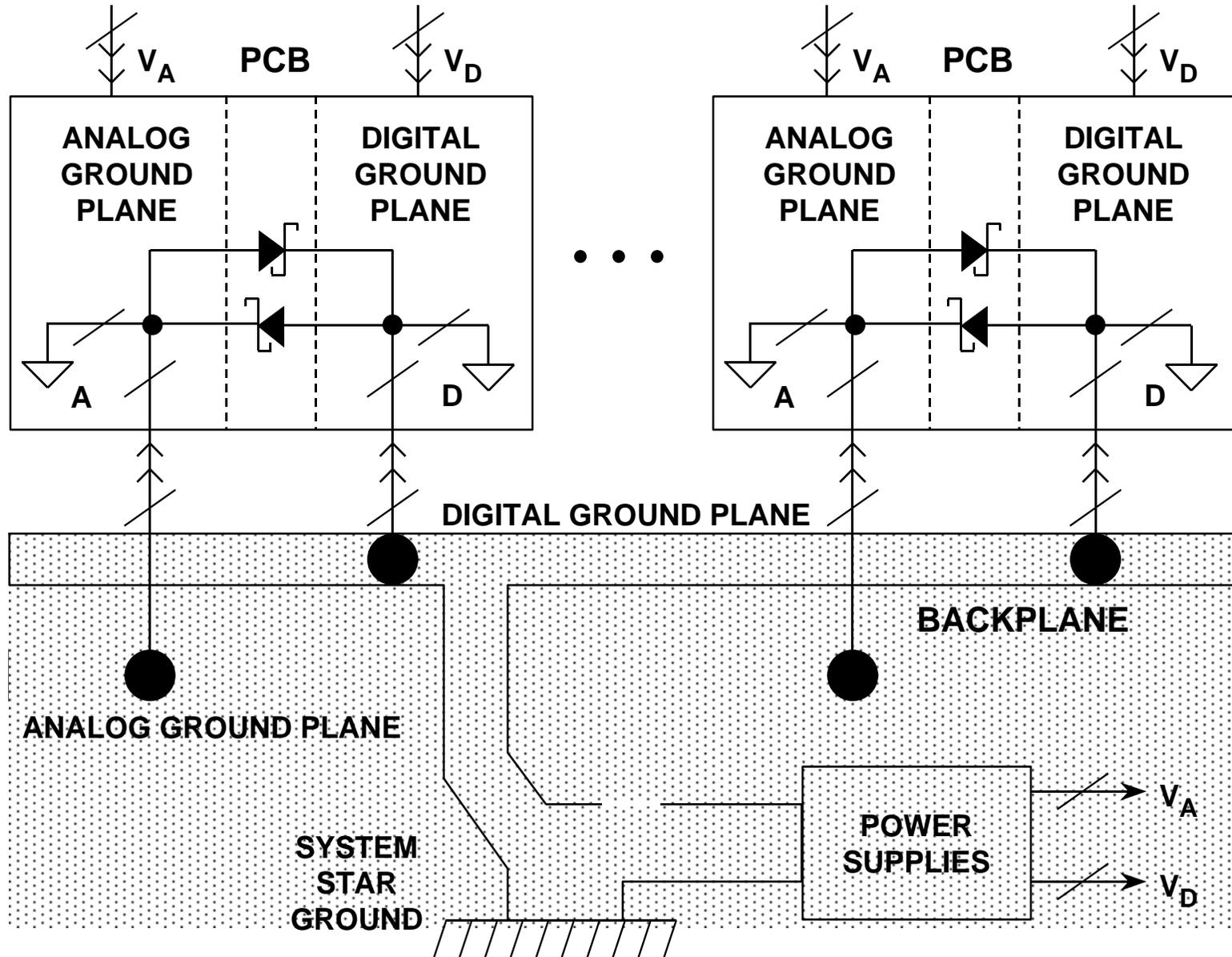
# MULTIPOINT GROUND CONCEPT



a

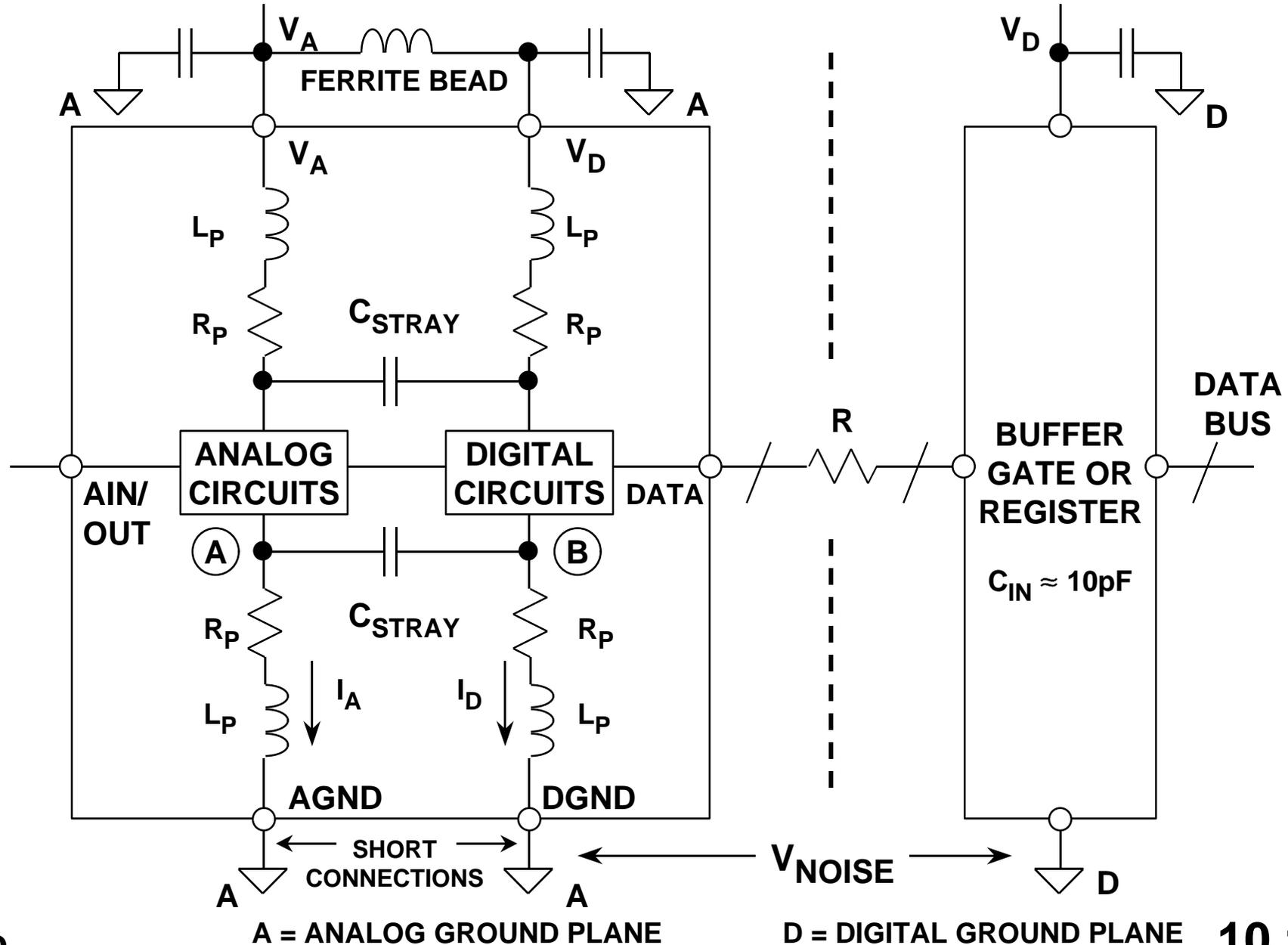
10.9

# SEPARATING ANALOG AND DIGITAL GROUND PLANES



a

# PROPER GROUNDING OF MIXED-SIGNAL ICs



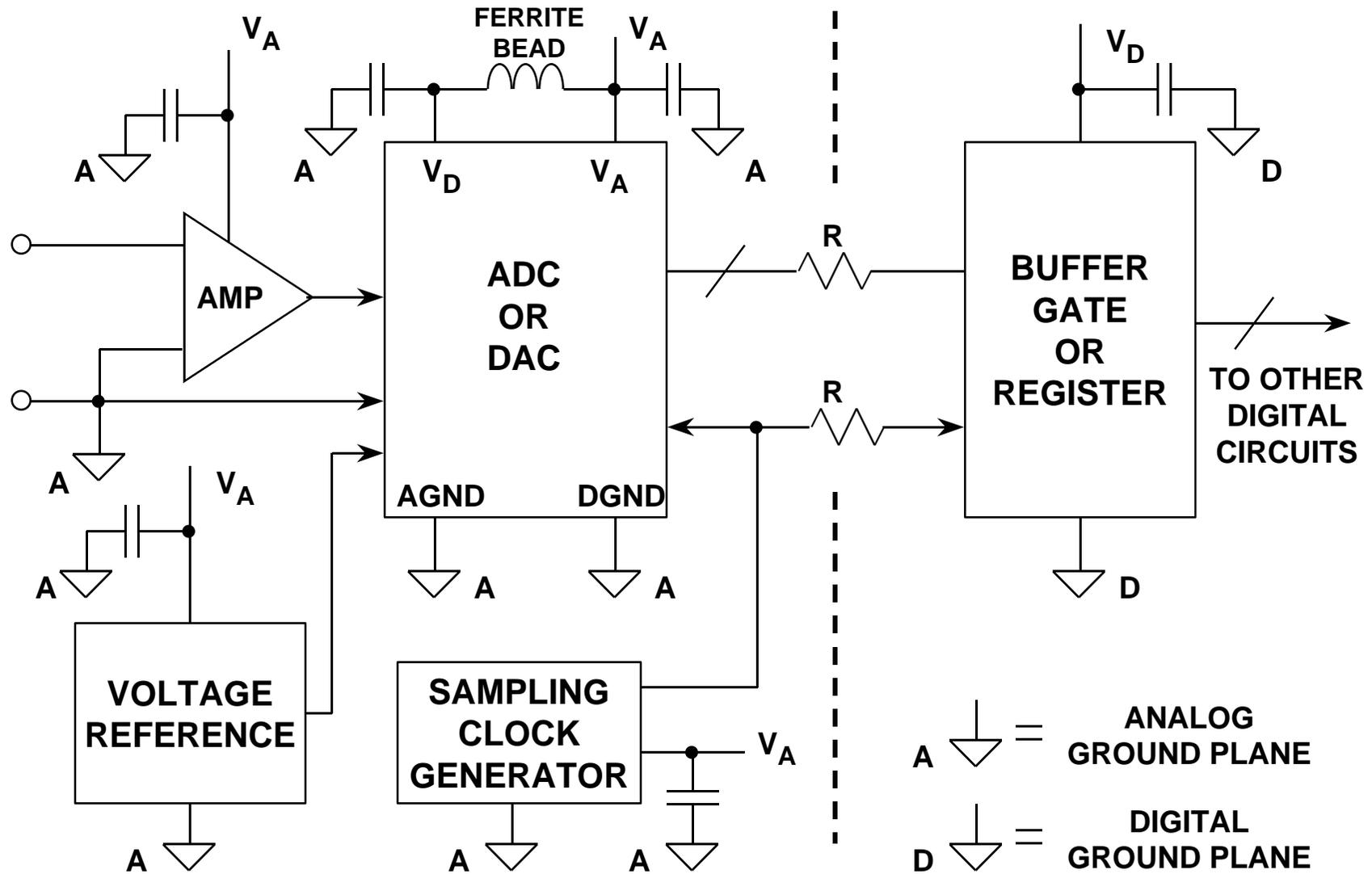
a

A = ANALOG GROUND PLANE

D = DIGITAL GROUND PLANE

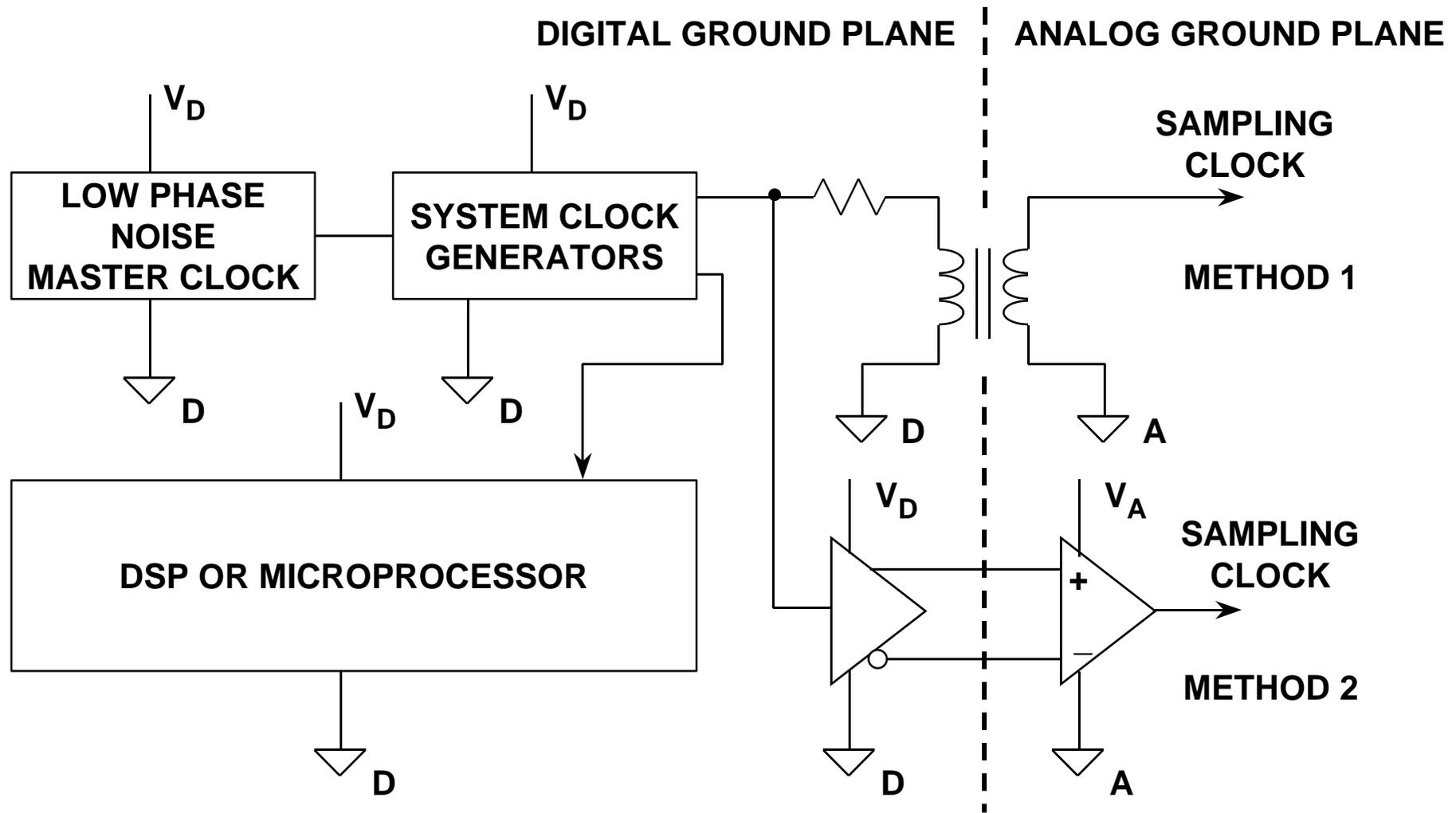
10.11

# GROUNDING AND DECOUPLING POINTS



a

# SAMPLING CLOCK DISTRIBUTION FROM DIGITAL TO ANALOG GROUND PLANES



$$SNR = 20 \log_{10} \left[ \frac{1}{2\pi f t_j} \right]$$

$t_j$  = Sampling Clock Jitter  
 $f$  = Analog Input Frequency

a



# SWITCHING REGULATOR NOISE REDUCTION TOOLS

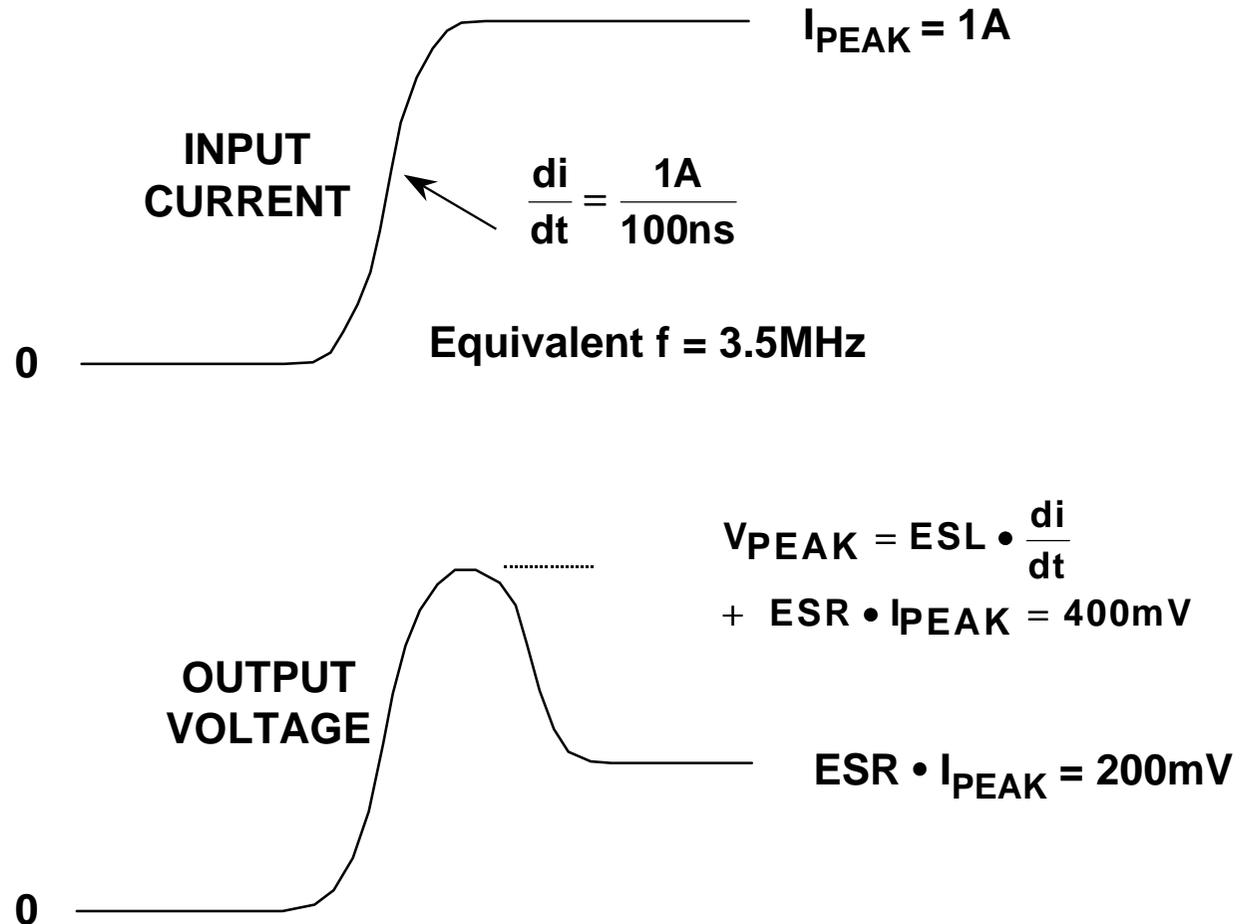
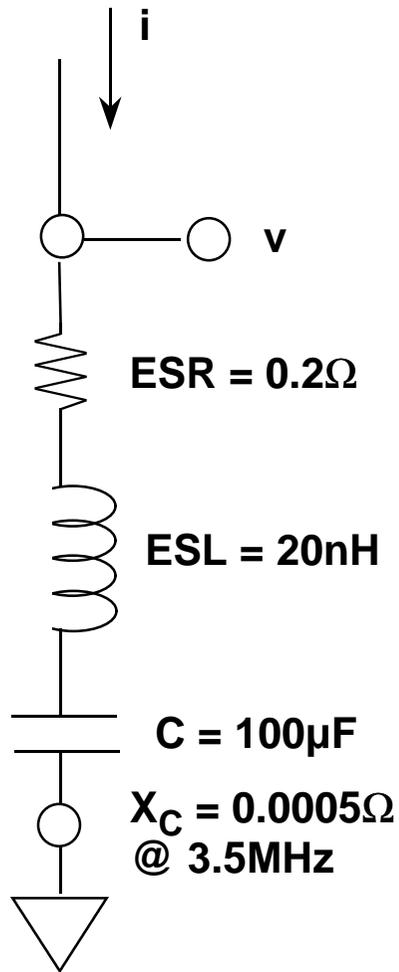
- Capacitors
- Inductors
- Ferrites
- Resistors
- Linear Post Regulation
- Proper Layout and Grounding Techniques
- **PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS!!**

# TYPES OF CAPACITORS

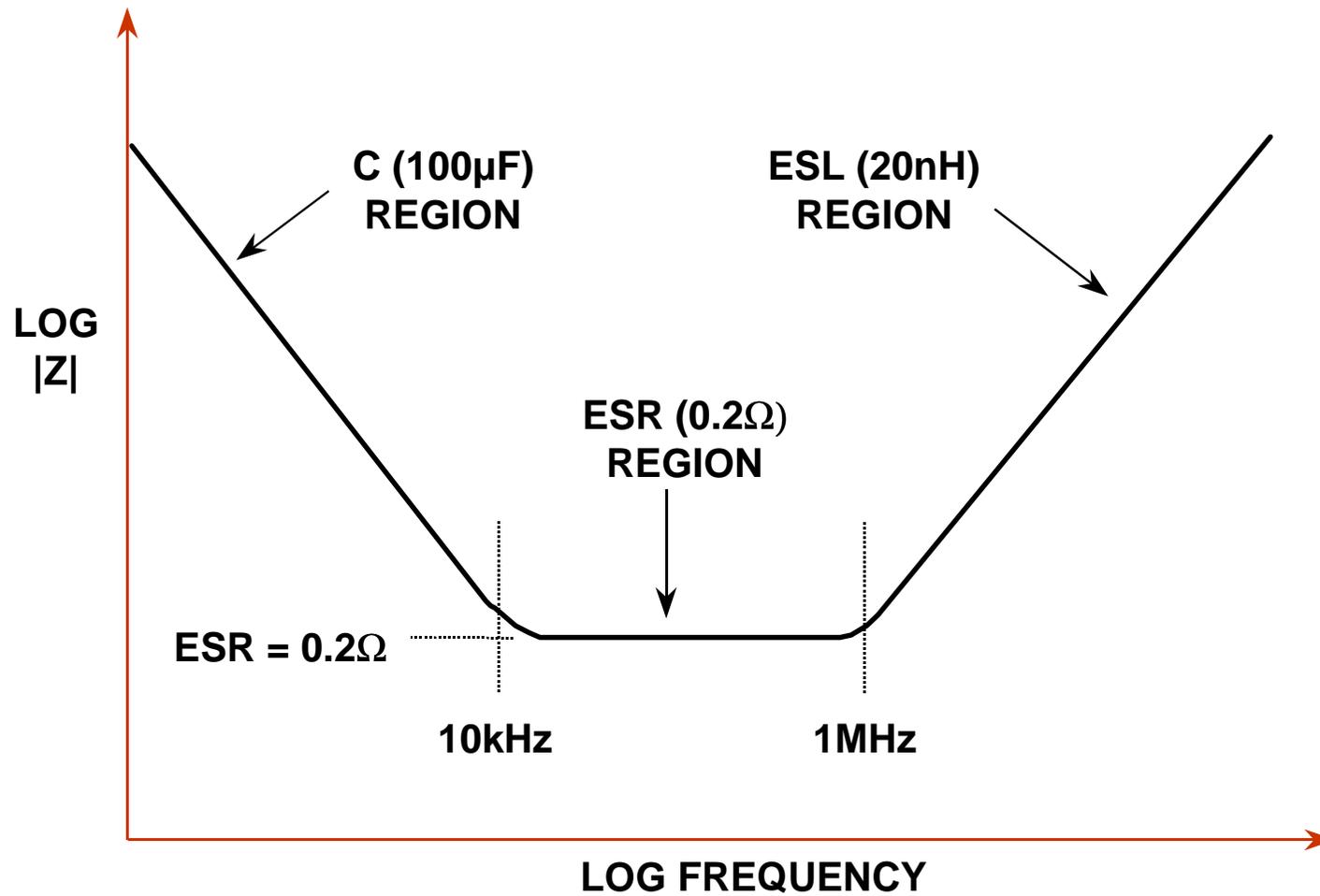
	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 $\mu\text{F}$	120 $\mu\text{F}$	120 $\mu\text{F}$	100 $\mu\text{F}$	1 $\mu\text{F}$	0.1 $\mu\text{F}$
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 $\Omega$ @ 100 kHz	0.18 $\Omega$ @ 100 kHz	0.12 $\Omega$ @ 100 kHz	0.02 $\Omega$ @ 100 kHz	0.11 $\Omega$ @ 1 MHz	0.12 $\Omega$ @ 1 MHz
Operating Frequency (*)	$\cong$ 100 kHz	$\cong$ 500 kHz	$\cong$ 1 MHz	$\cong$ 1 MHz	$\cong$ 10 MHz	$\cong$ 1 GHz

(\*) Upper frequency strongly size and package dependent

# CAPACITOR EQUIVALENT CIRCUIT AND PULSE RESPONSE



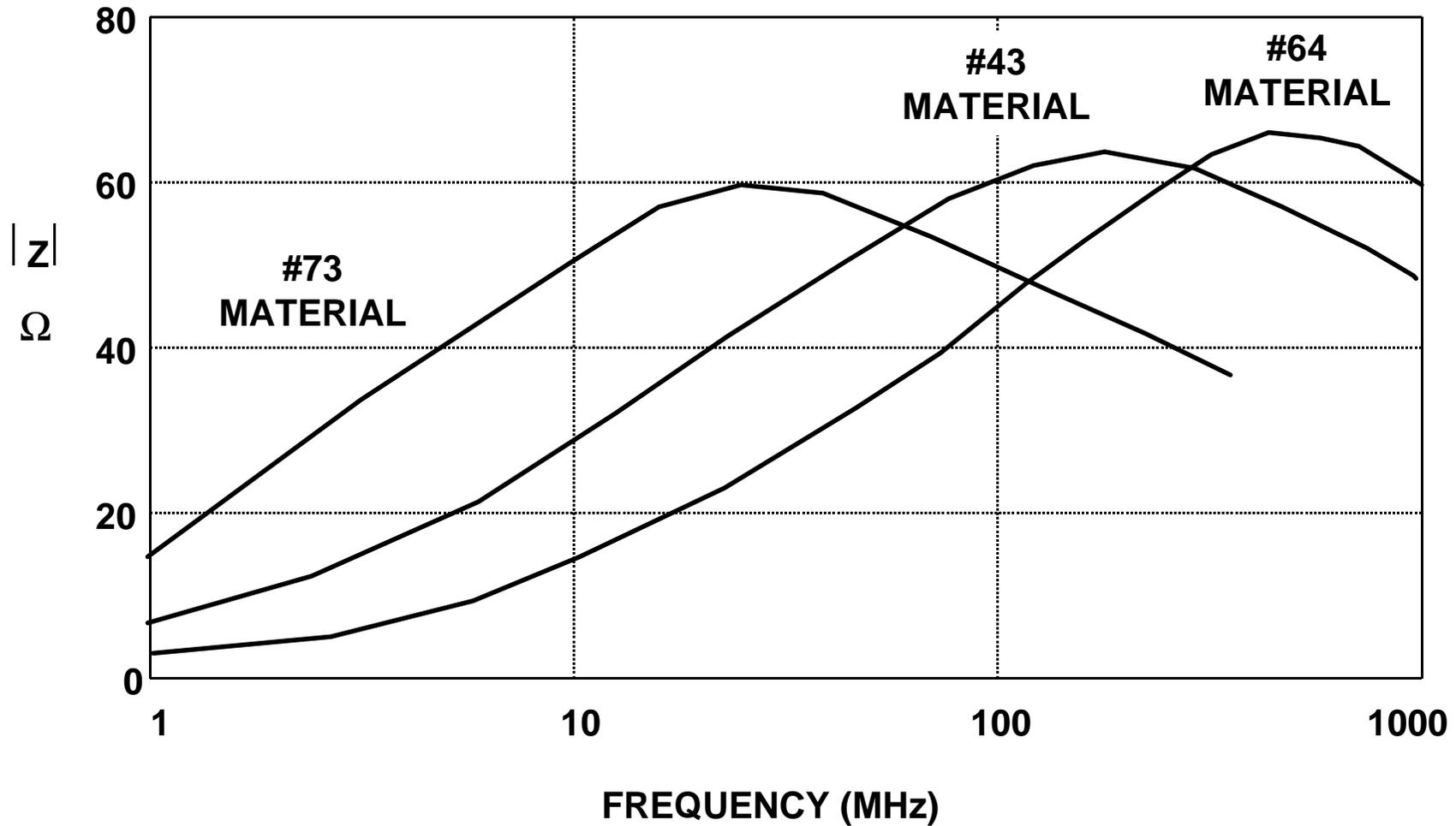
# ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY



# FERRITES SUITABLE FOR HIGH FREQUENCY FILTERS

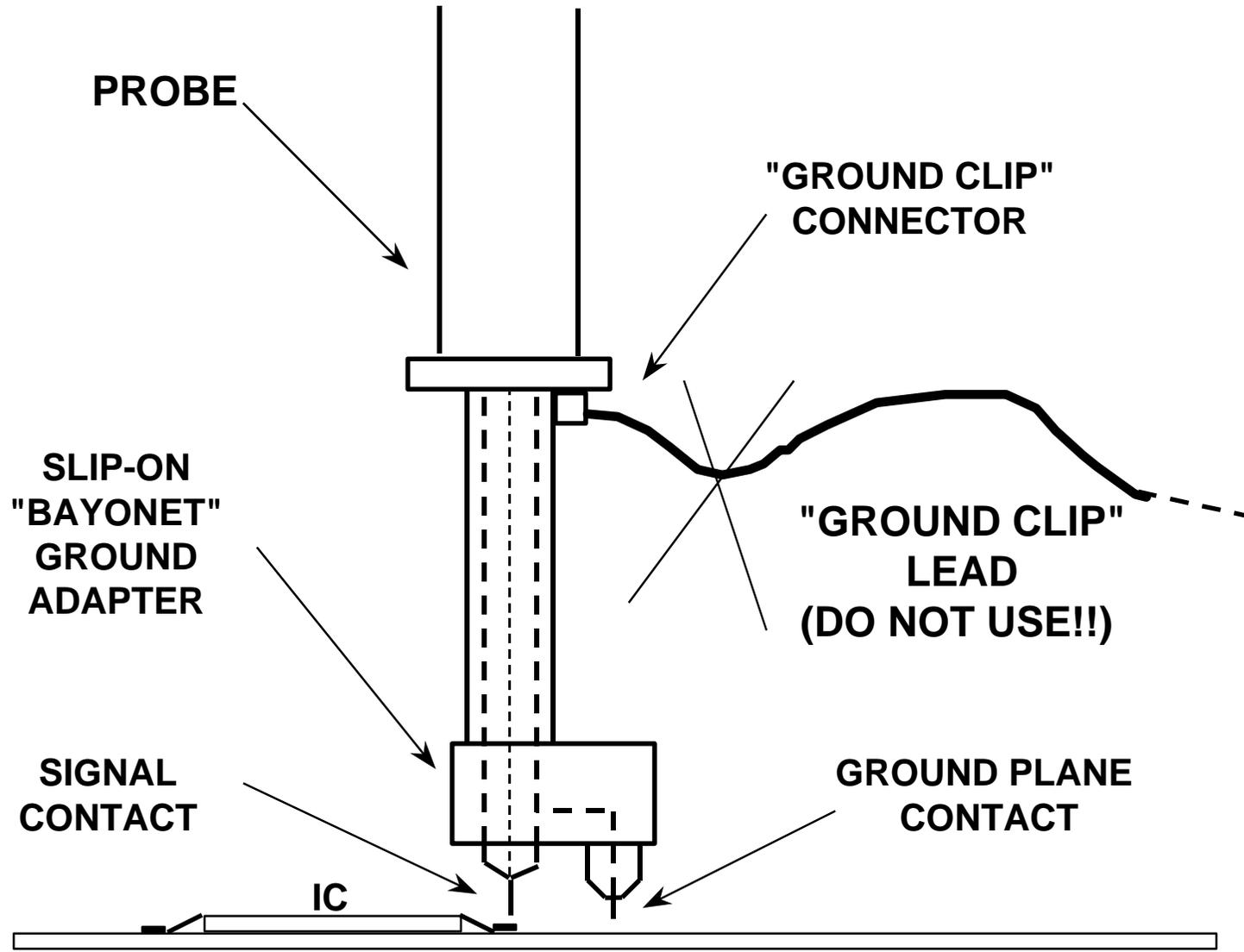
- Ferrites Good for Frequencies Above 25kHz
- Many Sizes and Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
  - ◆ Source and Frequency of Interference
  - ◆ Impedance Required at Interference Frequency
  - ◆ Environmental: Temperature, AC and DC Field Strength, Size / Space Available
- Always Test the Design!

# IMPEDANCE OF FERRITE BEADS



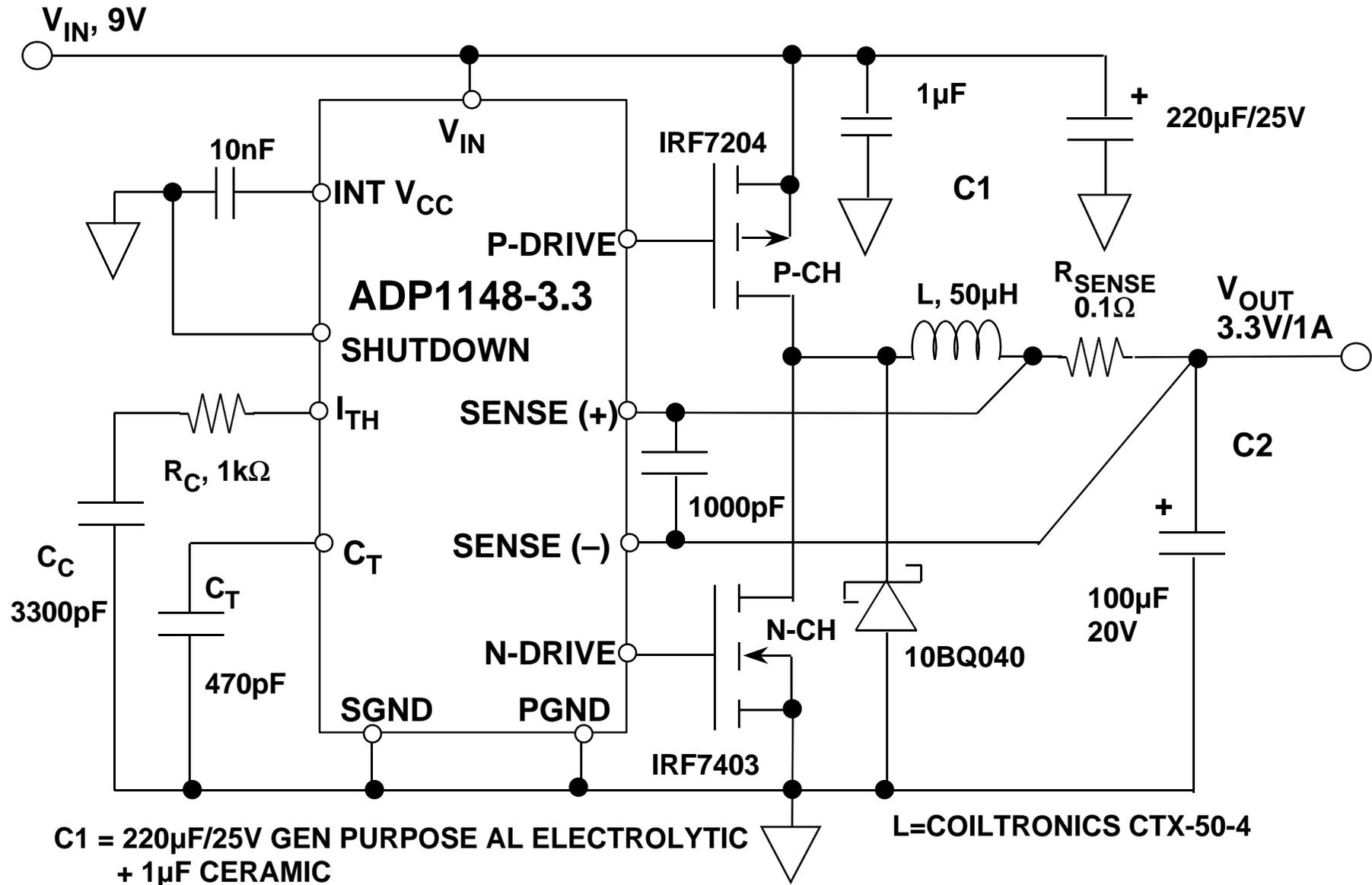
Courtesy: Fair-Rite Products Corp, Wallkill, NY  
(<http://www.fair-rite.com>)

# PROPER PROBING TECHNIQUES



a

# ADP1148 BUCK REGULATOR CIRCUIT



C1 = 220µF/25V GEN PURPOSE AL ELECTROLYTIC  
+ 1µF CERAMIC

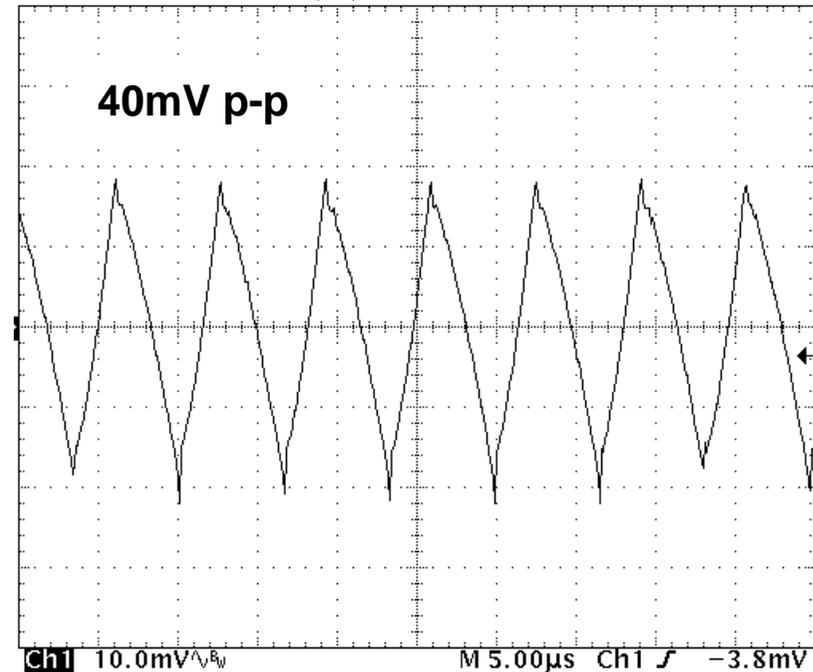
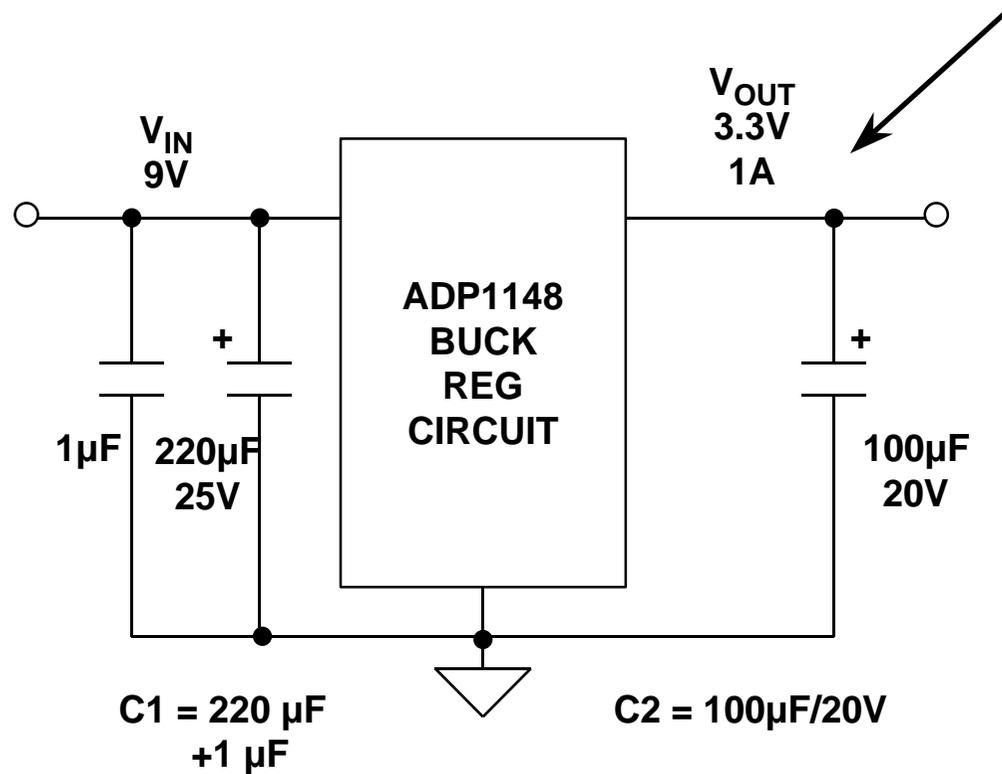
L=COILTRONICS CTX-50-4

C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES, ESR = 0.6Ω

10.22

a

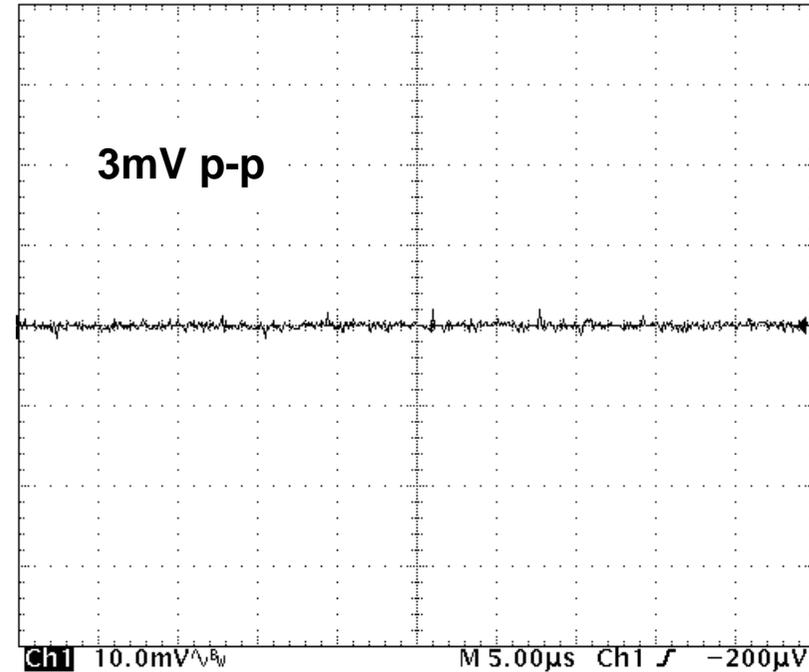
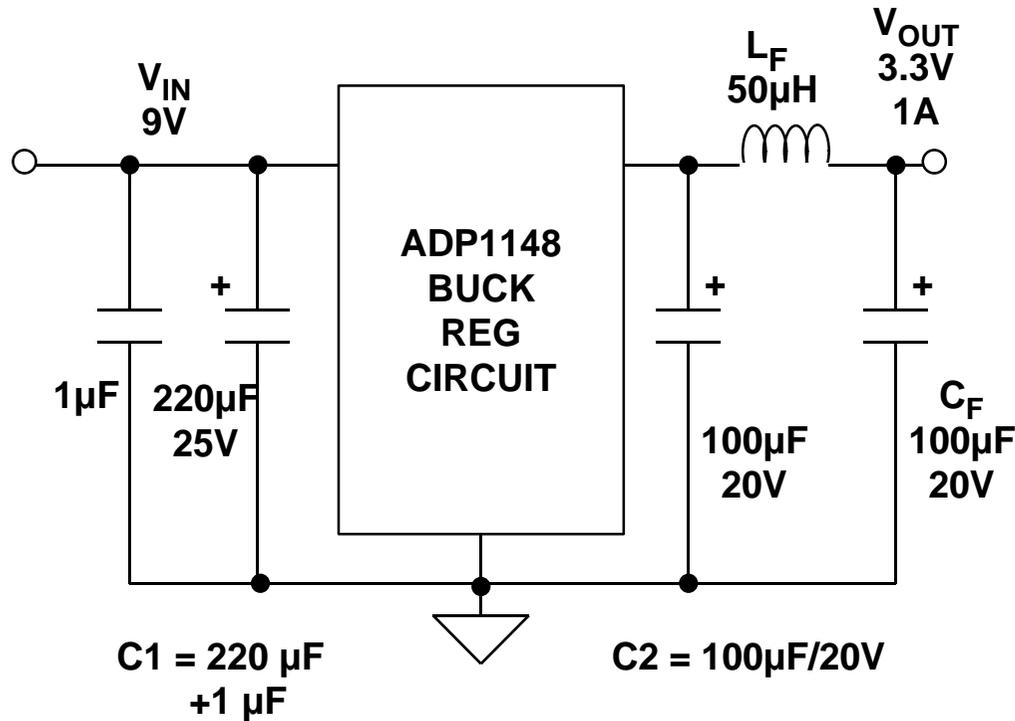
# ADP1148 BUCK OUTPUT WAVEFORM



VERTICAL SCALE: 10mV / DIV  
HORIZ. SCALE: 5µs / DIV

C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC  
C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)

# ADP1148 BUCK FILTERED OUTPUT



**VERTICAL SCALE: 10mV / DIV**  
**HORIZ. SCALE: 5µs / DIV**

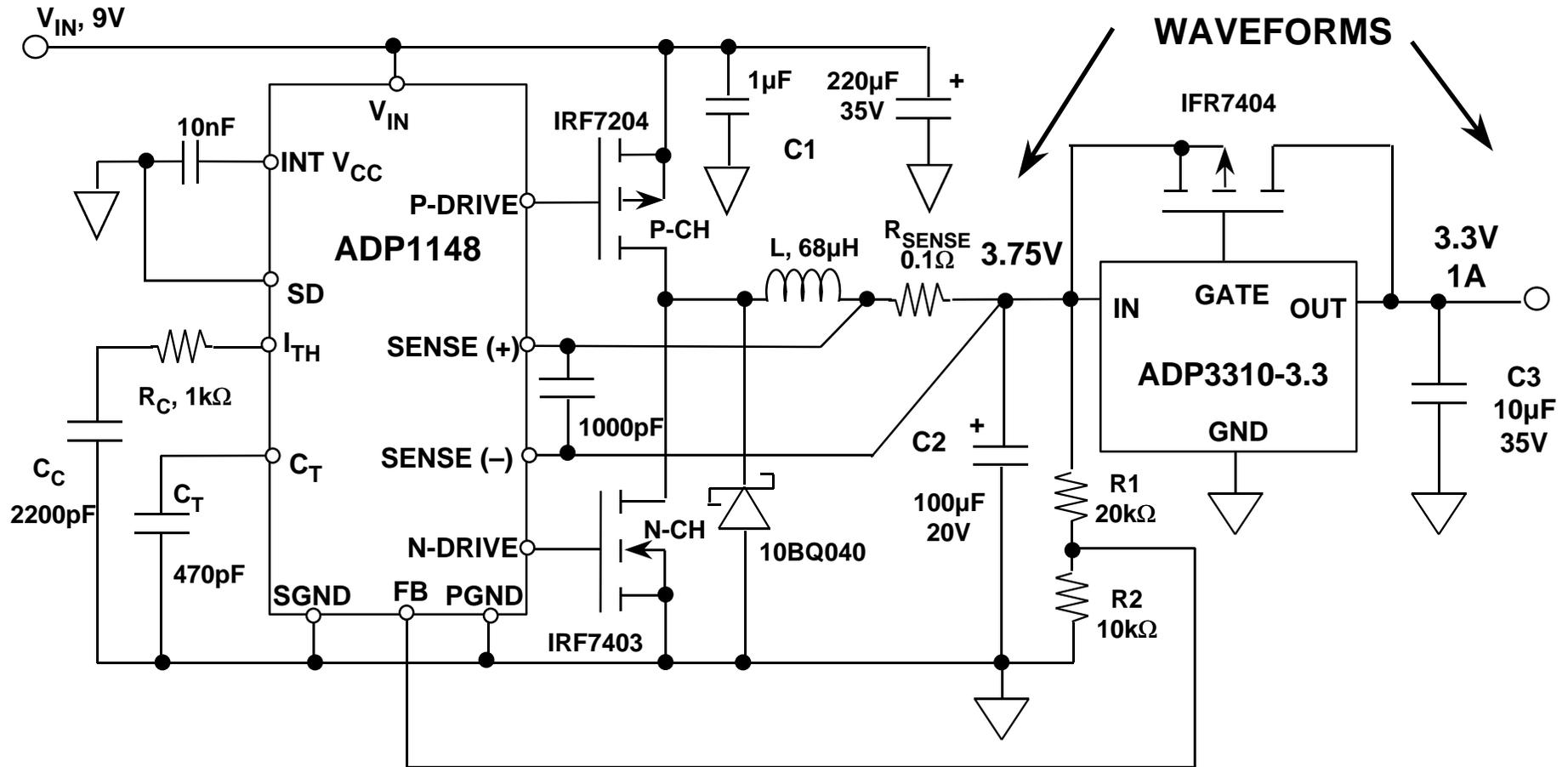
**C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC**  
**C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)**

**OUTPUT FILTER**

**L<sub>F</sub> = COILTRONICS CTX-50-4**

**C<sub>F</sub> = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES**

# ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

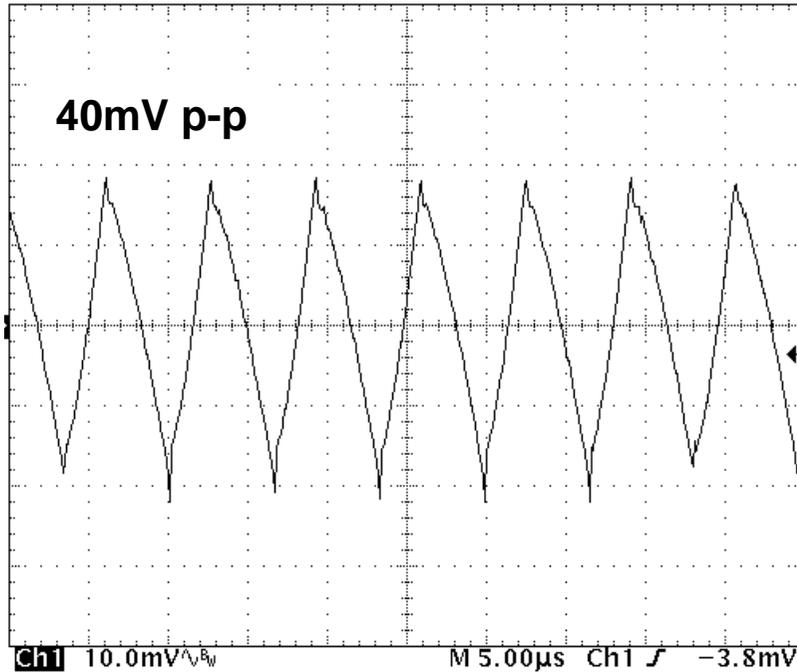


a

10.25

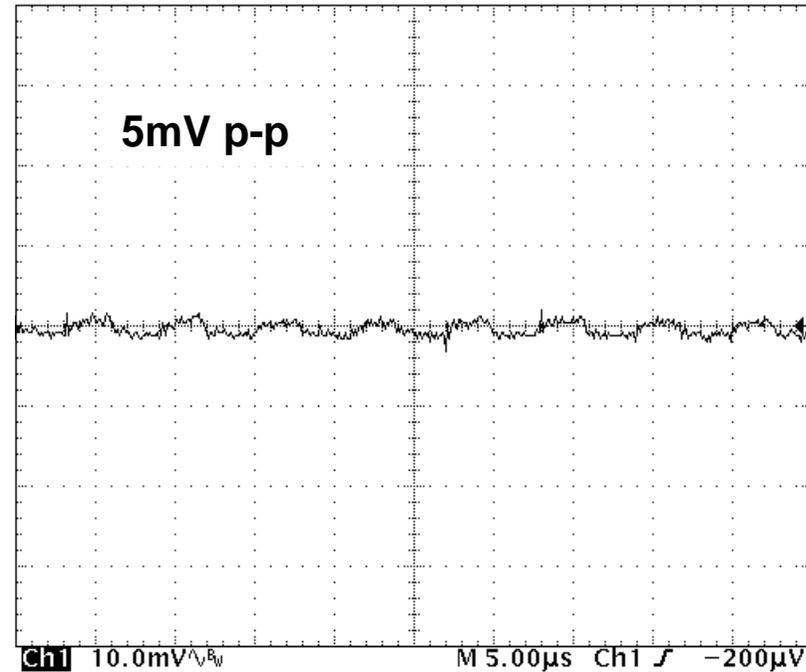
# WAVEFORMS FOR ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

ADP1148 OUTPUT  
(ADP3310 INPUT)



VERTICAL SCALE: 10mV/DIV  
HORIZ. SCALE: 5μs/DIV

ADP3310 OUTPUT

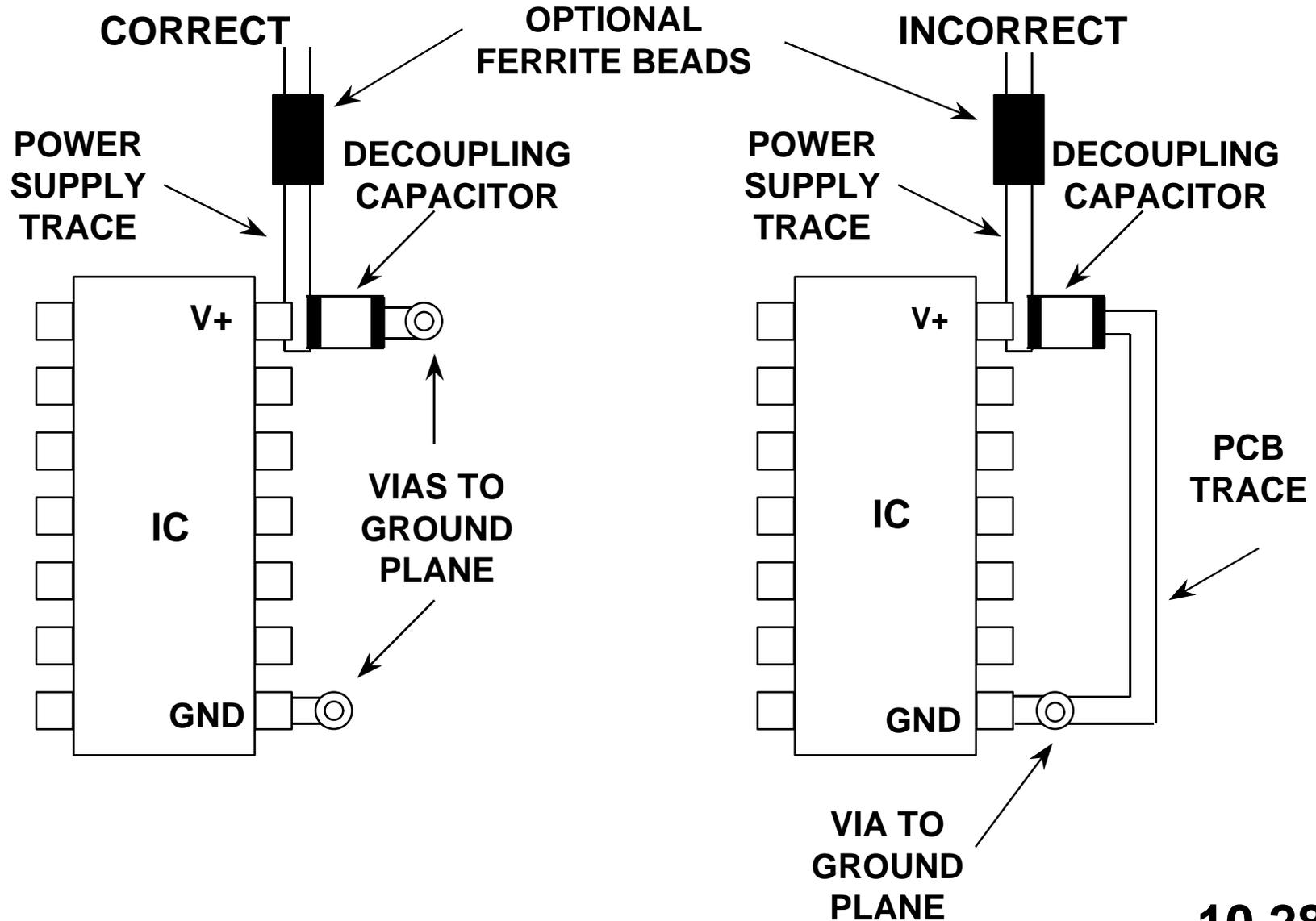


VERTICAL SCALE: 10mV/DIV  
HORIZ. SCALE: 5μs/DIV

# SWITCHING SUPPLY FILTER SUMMARY

- **Proper Layout and Grounding (using Ground Plane) Mandatory**
- **Low ESL/ESR Capacitors Give Best Results**
- **Parallel Capacitors Lower ESR/ESL and Increase Capacitance**
- **External LC Filters Very Effective in Reducing Ripple**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results**
- **Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit**
- **High Frequency Localized Decoupling at IC Power Pins is Still Required**

# LOCALIZED DECOUPLING TO GROUND PLANE USING SHORTEST PATH

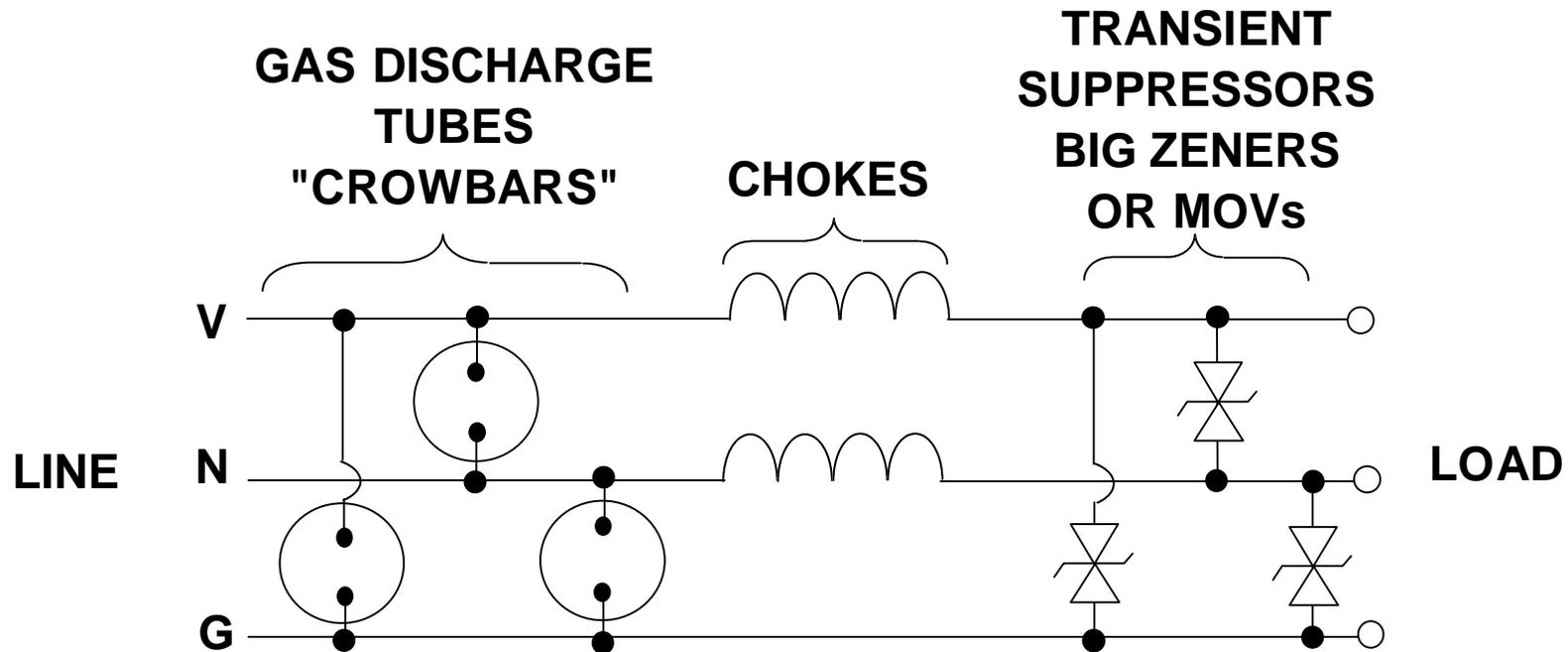


a

10.28

# POWER LINE DISTURBANCES CAN GENERATE EMI

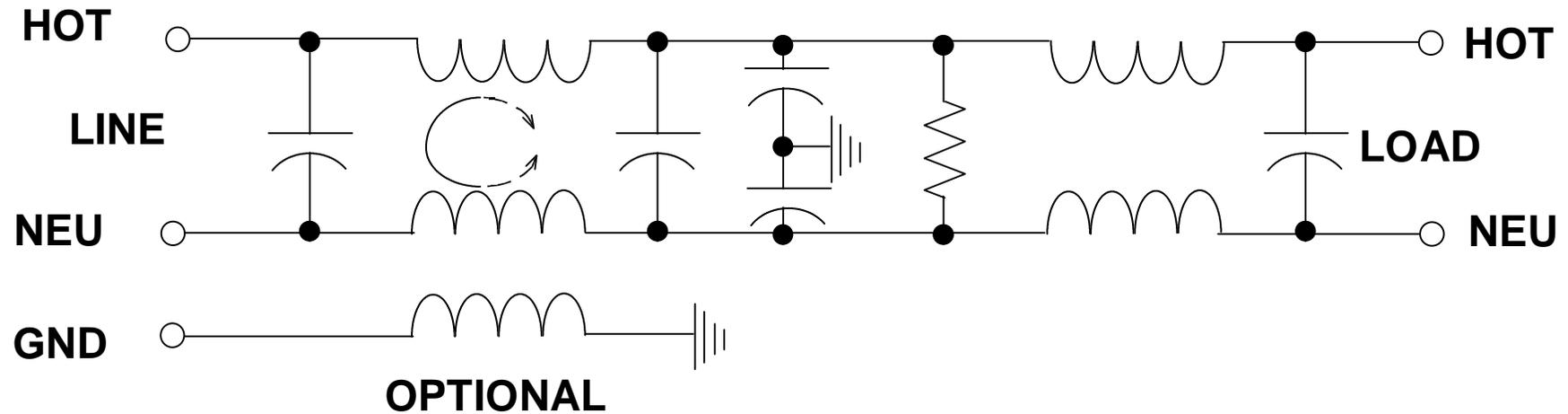
Reprinted from EDN Magazine (January 20, 1994), © CAHNERS PUBLISHING COMPANY 1995, A Division of Reed Publishing USA



■ COMMON-MODE AND DIFFERENTIAL MODE PROTECTION

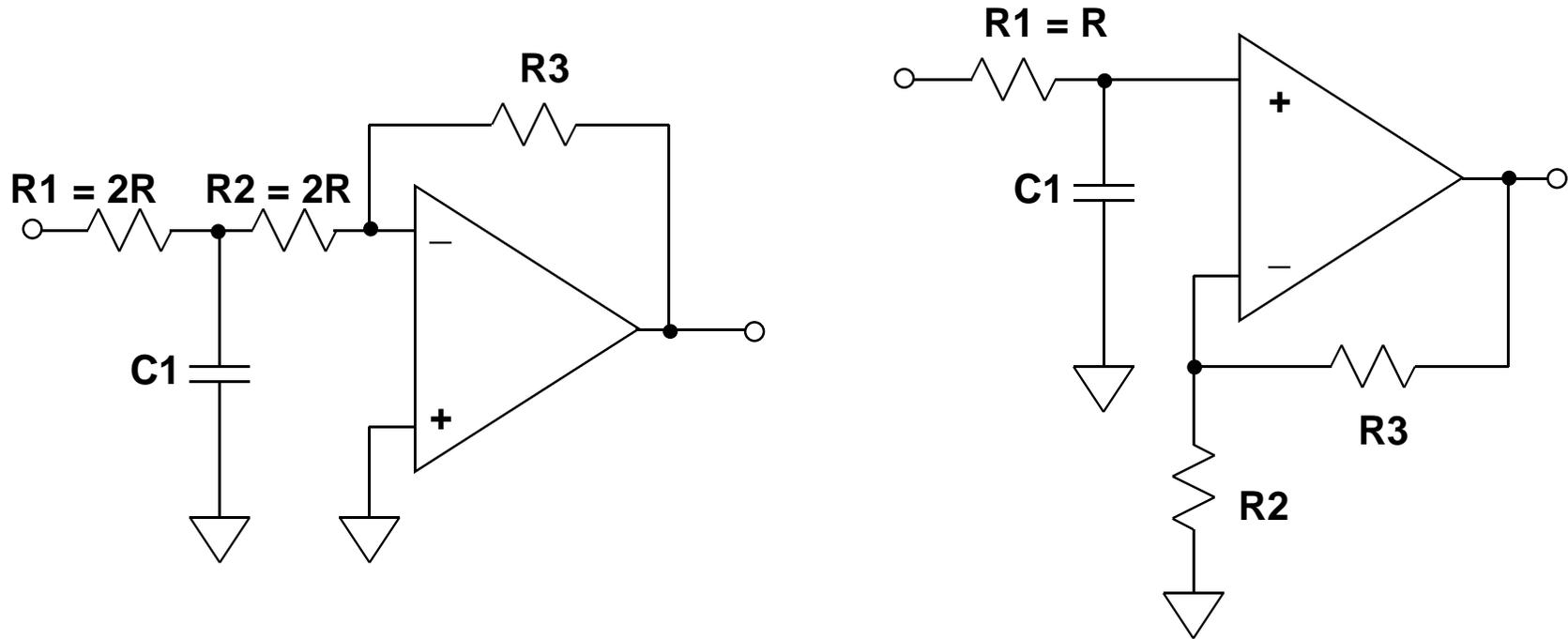
# SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER

Reprinted from EDN Magazine (January 20, 1994), © CAHNERS PUBLISHING COMPANY 1995, A Division of Reed Publishing USA



**NOTE: OPTIONAL CHOKE ADDED FOR COMMON-MODE PROTECTION**

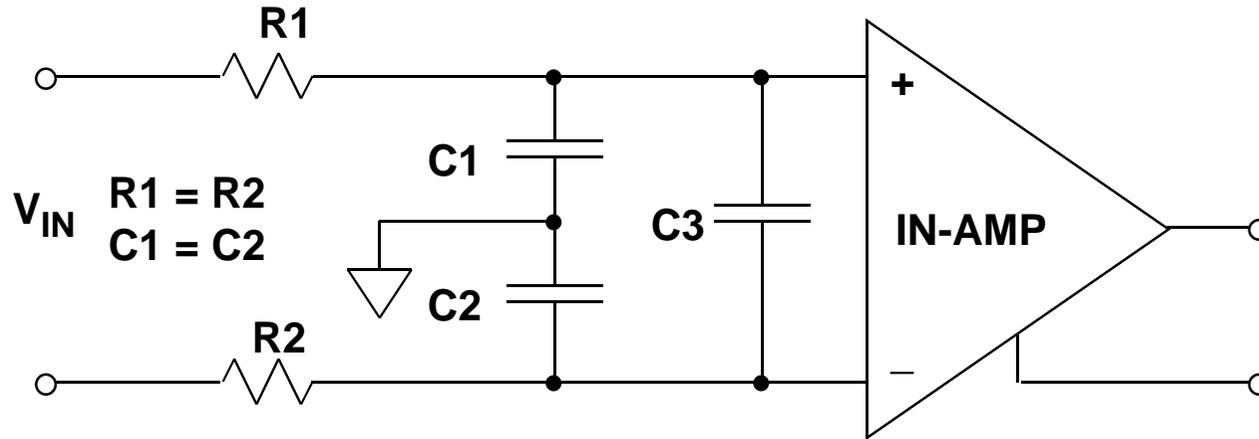
# FILTERING AMPLIFIER INPUTS TO PREVENT RFI RECTIFICATION



$$\text{FILTER BANDWIDTH} = \frac{1}{2\pi R C1}$$

> 100 × SIGNAL BANDWIDTH

# FILTERING IN-AMP INPUTS



$$\tau_{DIFF} = (R1 + R2) C3$$

$$\tau_{CM} = R1 \cdot C1 = R2 \cdot C2 \quad \tau_{DIFF} \gg \tau_{CM}$$

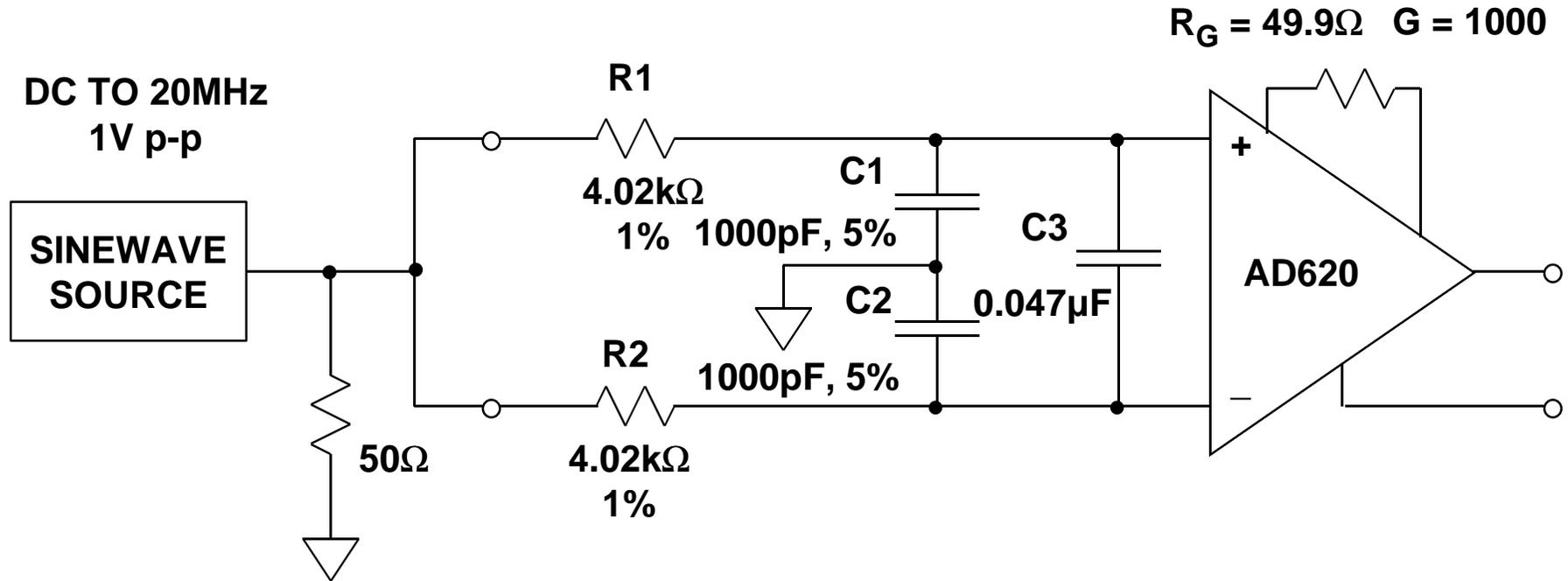
**R1·C1 SHOULD MATCH R2·C2**

**R1 = R2 SHOULD BE 1% RESISTORS**

**C1 = C2 SHOULD BE 5% CAPACITORS**

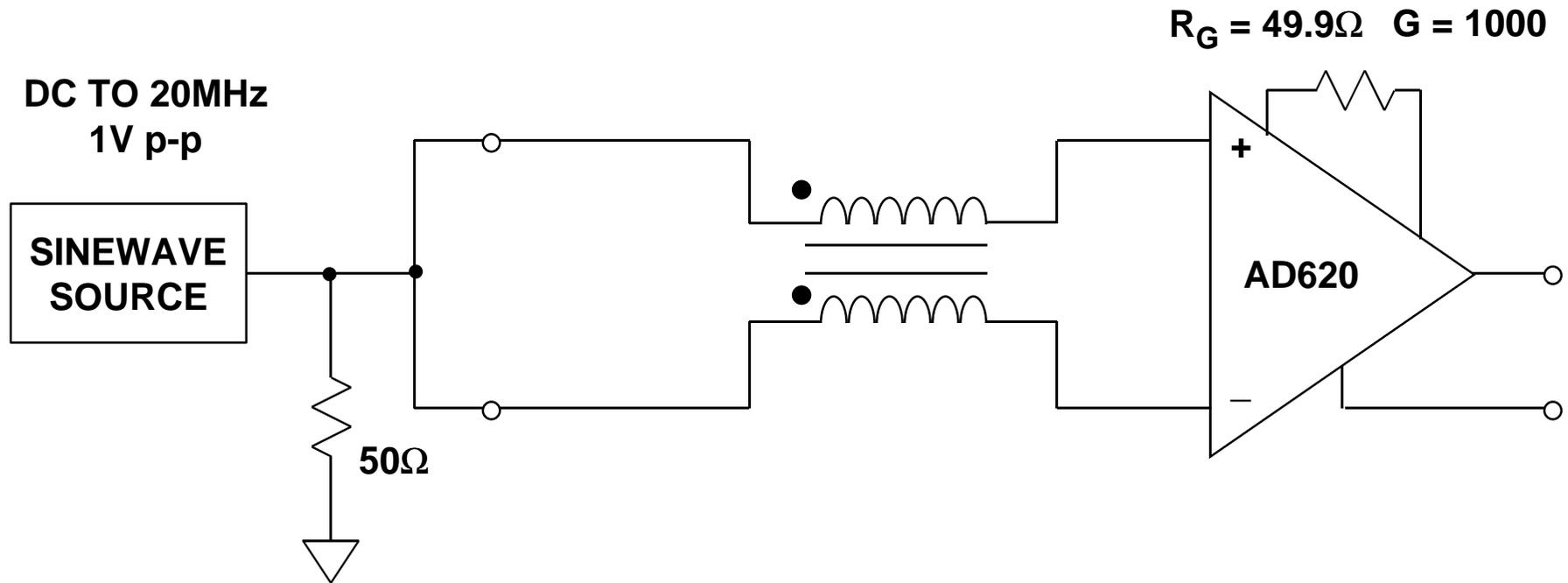
$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2) \left[ \frac{C1 \cdot C2}{C1 + C2} + C3 \right]}$$

# COMMON AND DIFFERENTIAL MODE FILTER WITH AD620



- FILTER BANDWIDTH  $\approx 400\text{Hz}$
- OFFSET SHIFT RTI  $< 1.5\ \mu\text{V}$

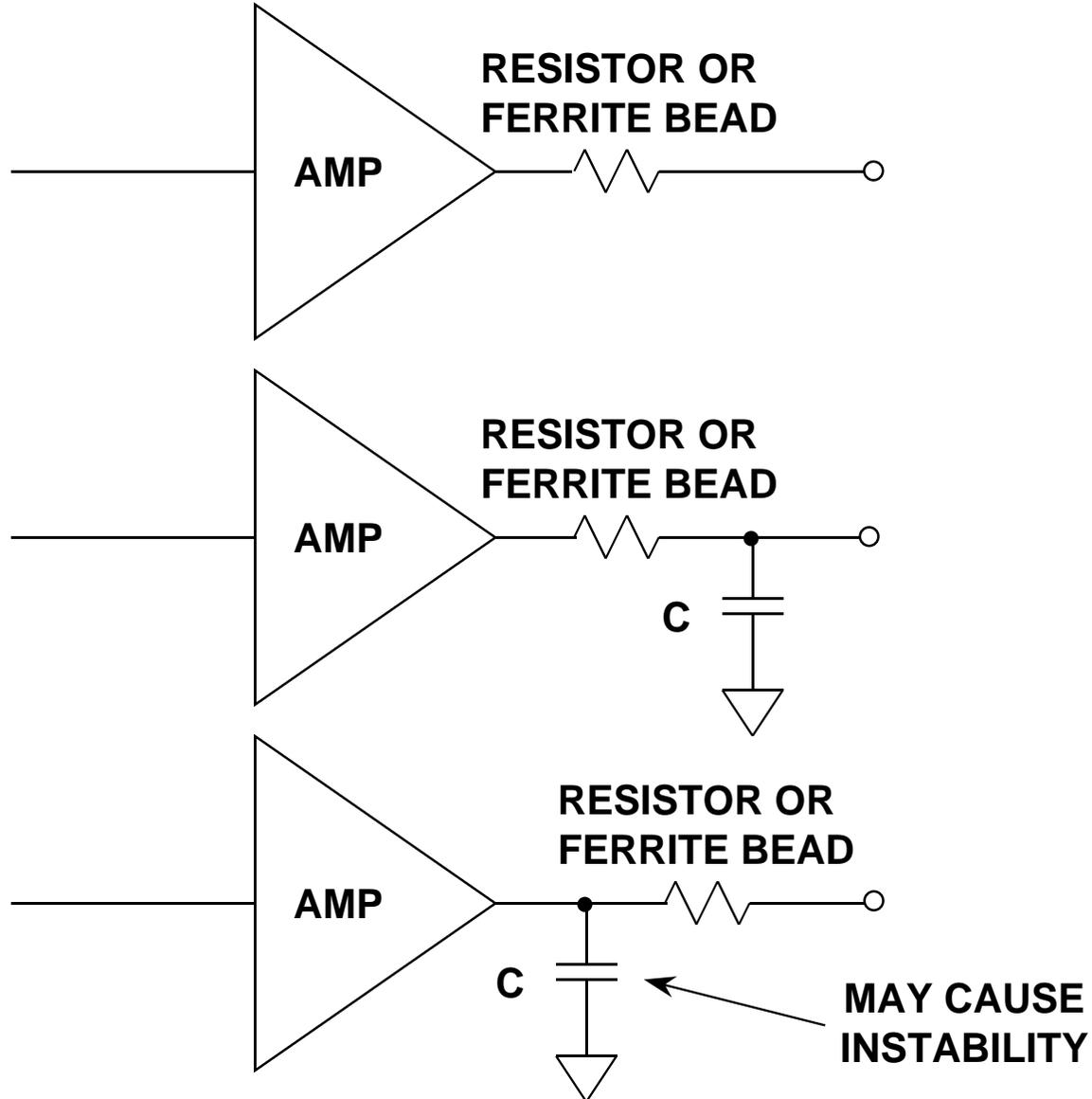
# COMMON MODE CHOKE WITH AD620



■ **COMMON MODE CHOKE:**  
PULSE ENGINEERING B4001  
<http://www.pulseeng.com>

■ **OFFSET SHIFT RTI < 4.5 μV**

# FILTERING AMPLIFIER OUTPUTS PROTECTS AGAINST EMI/RFI EMISSION AND SUSCEPTIBILITY



a

# LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches/ns

Reprinted from EDN Magazine (January 20, 1994), © CAHNERS PUBLISHING COMPANY 1995, A Division of Reed Publishing USA

DIGITAL IC FAMILY	$t_r, t_s$ (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

$t_r$  = rise time of signal in ns

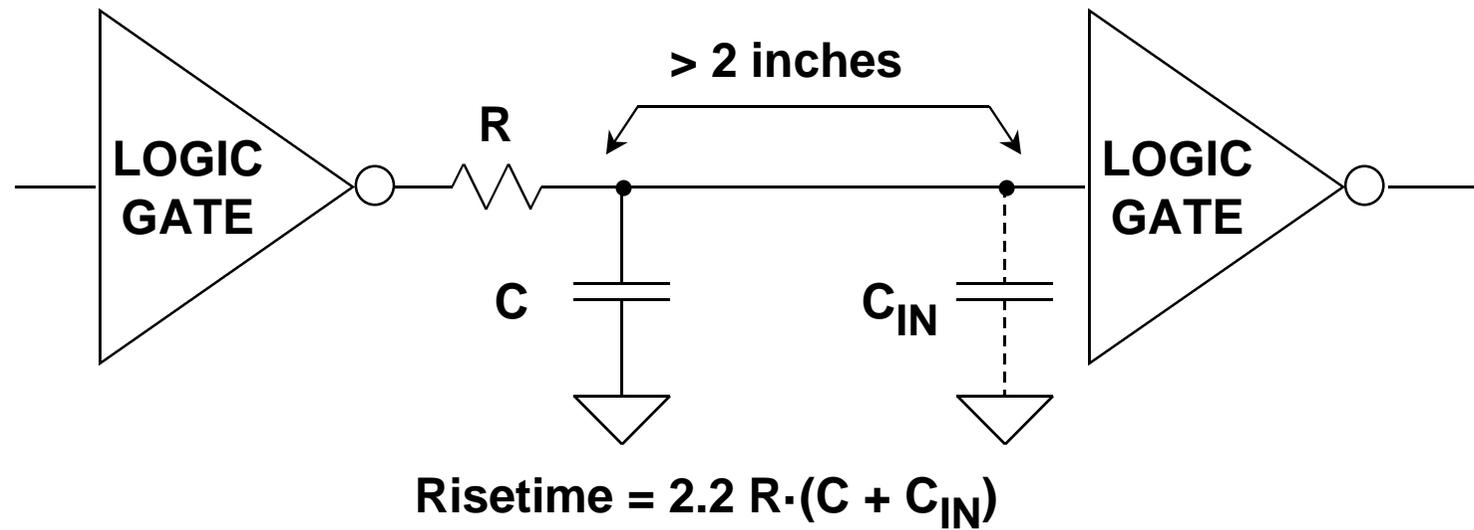
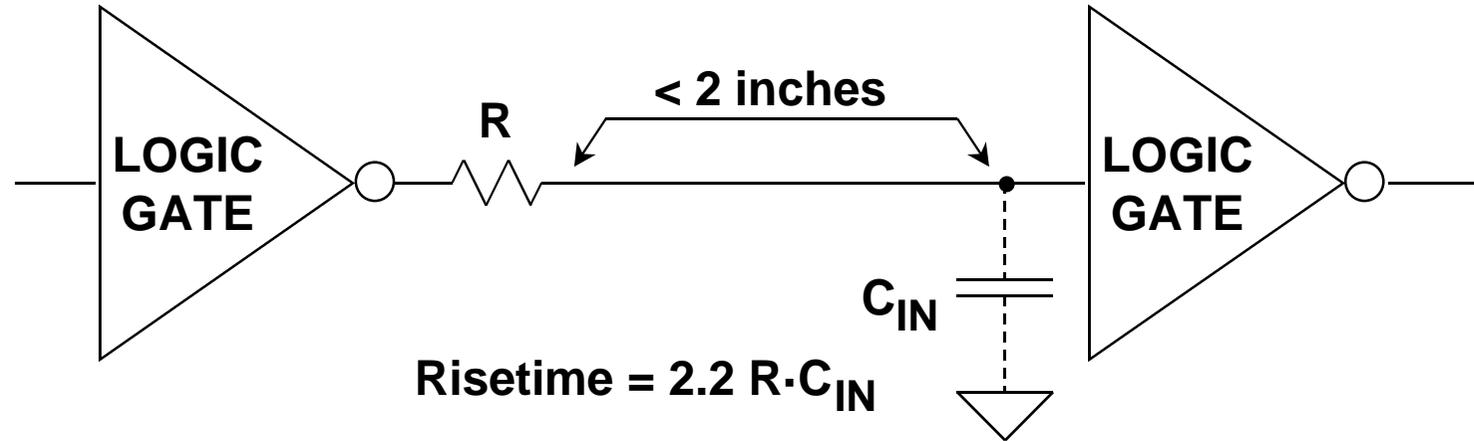
$t_f$  = fall time of signal in ns

For analog signals @  $f_{max}$ , calculate  $t_r = t_f = 0.35 / f_{max}$

a

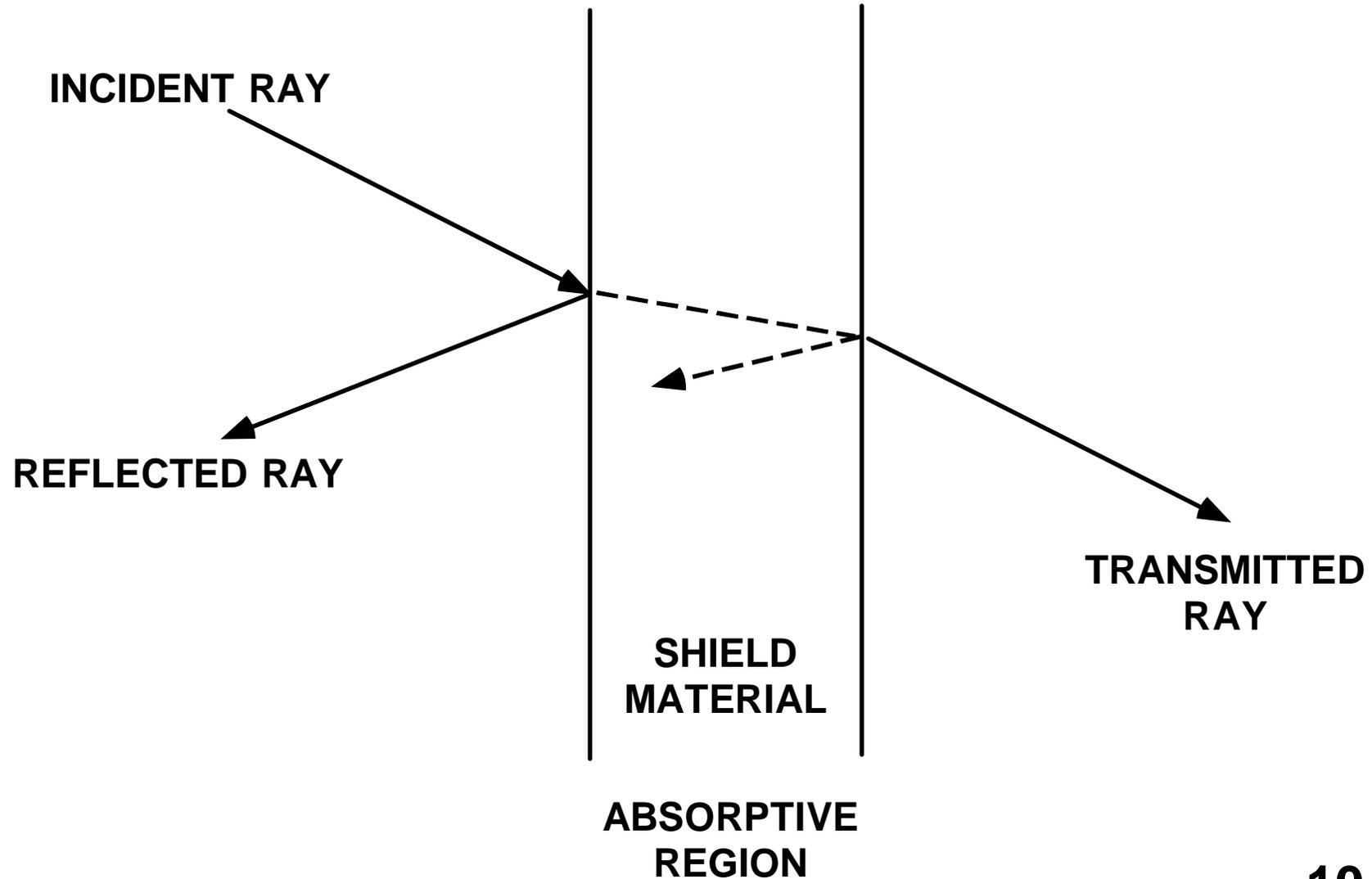
**10.36**

# SLOW DOWN FAST LOGIC EDGES TO MINIMIZE EMI/RFI PROBLEMS



# REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS

Reprinted from EDN Magazine (January 20, 1994), © CAHNERS PUBLISHING COMPANY 1995, A Division of Reed Publishing USA



a

10.38

## CONDUCTIVITY AND PERMEABILITY FOR VARIOUS SHIELDING MATERIALS

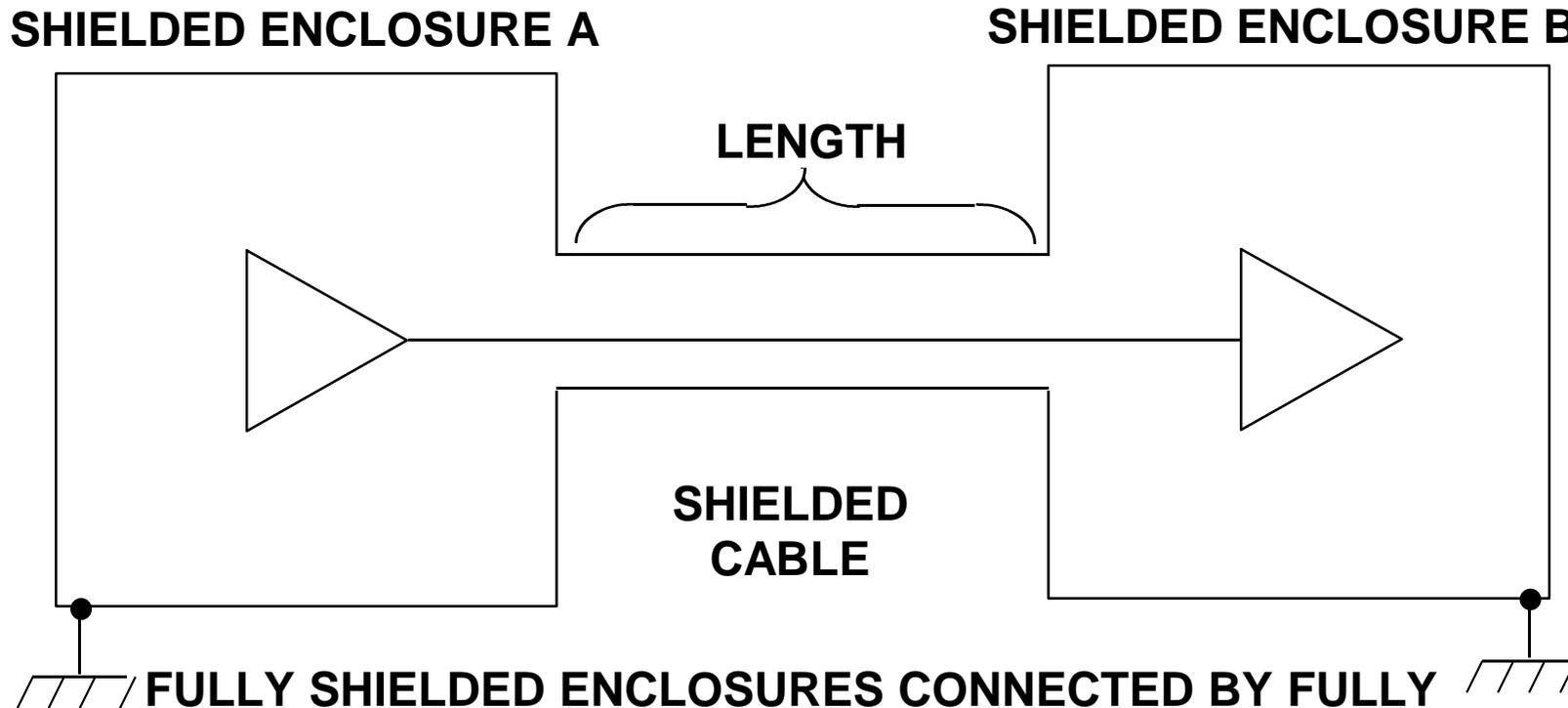
MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

**Conductivity: Ability to Conduct Electricity**

**Permeability: Ability to Absorb Magnetic Energy**

# "ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION

Reprinted from EDN Magazine (January 20, 1994), © CAHNERS PUBLISHING COMPANY 1995, A Division of Reed Publishing USA

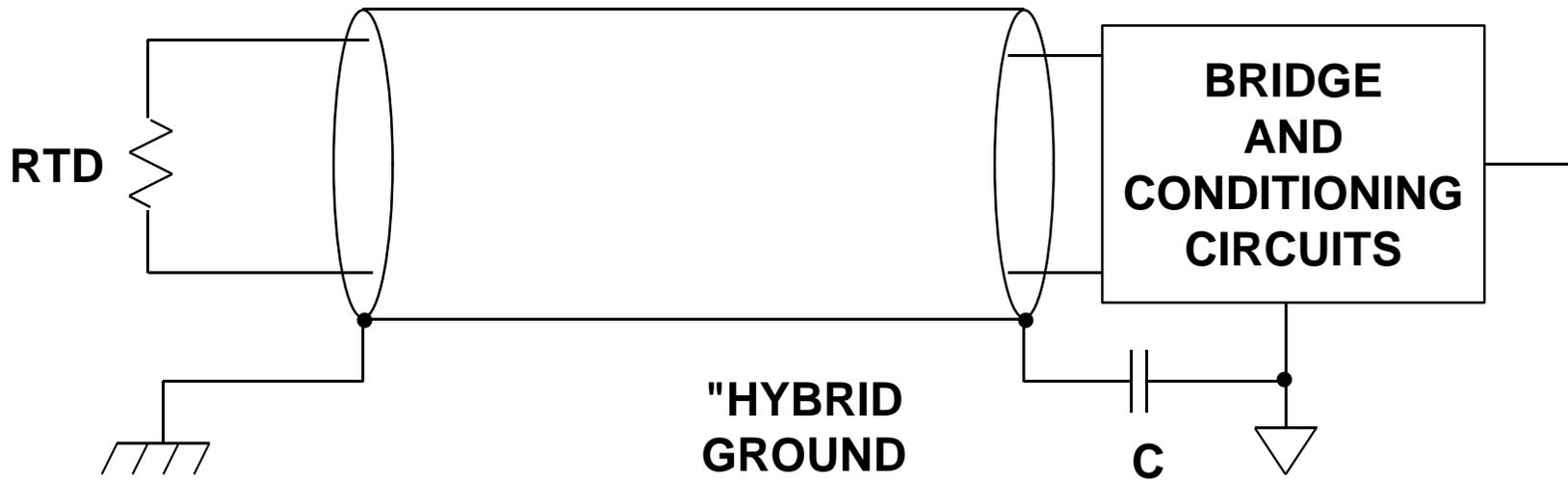
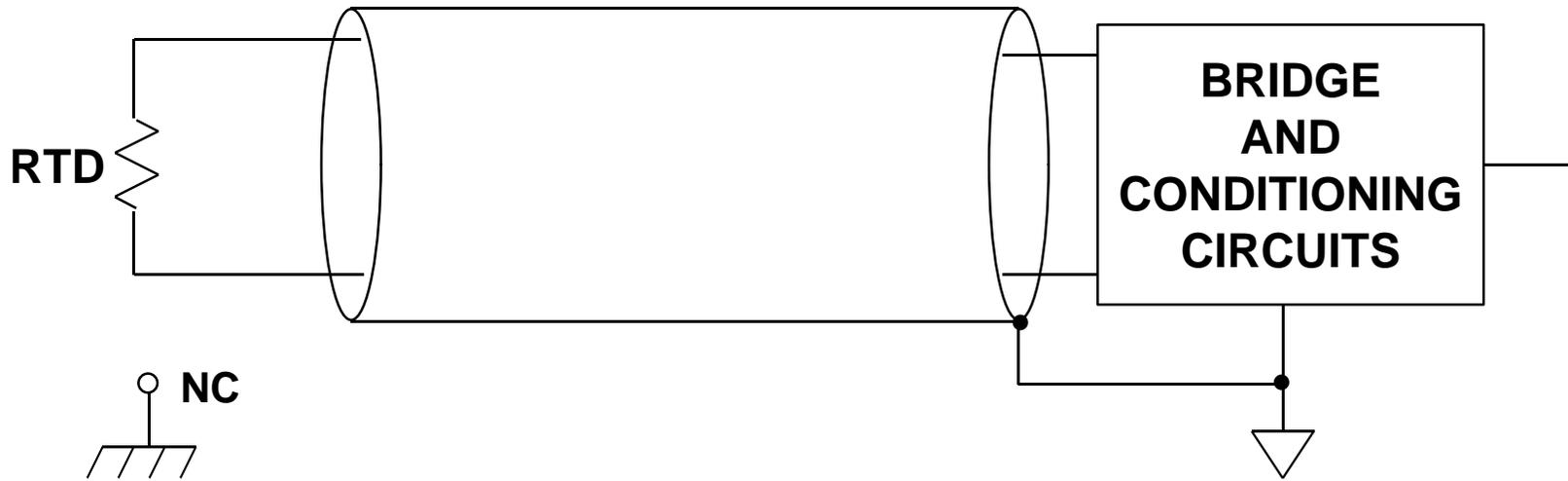


**FULLY SHIELDED ENCLOSURES CONNECTED BY FULLY SHIELDED CABLE KEEP ALL INTERNAL CIRCUITS AND SIGNAL LINES INSIDE THE SHIELD.**

- **TRANSITION REGION:  $1/20$  WAVELENGTH**

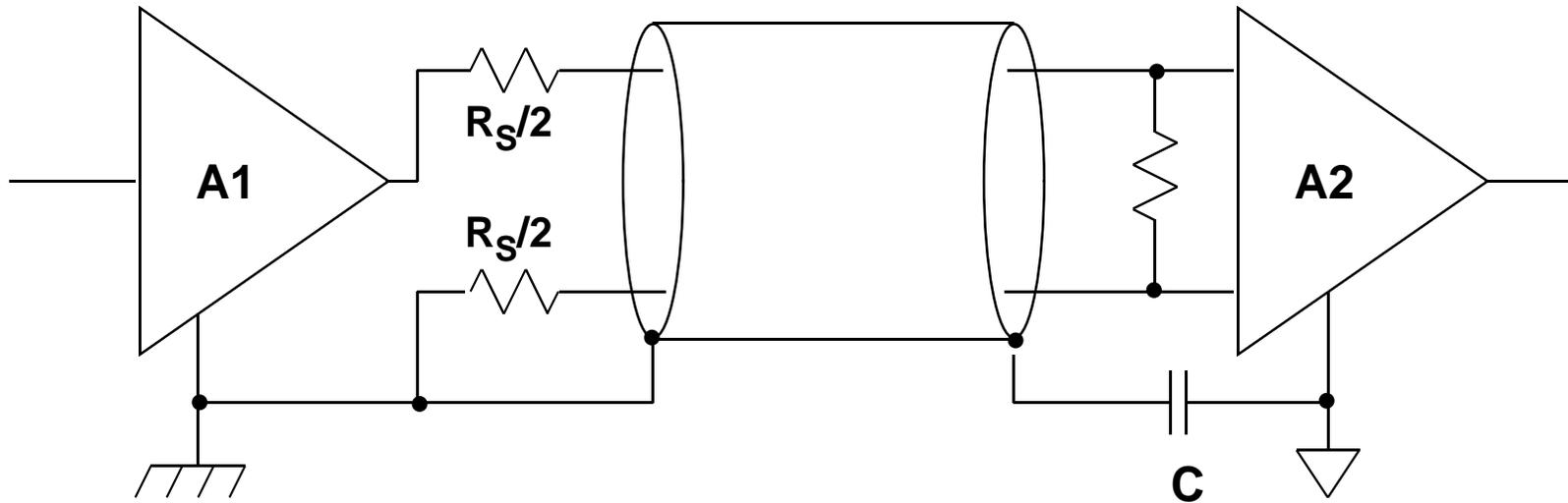
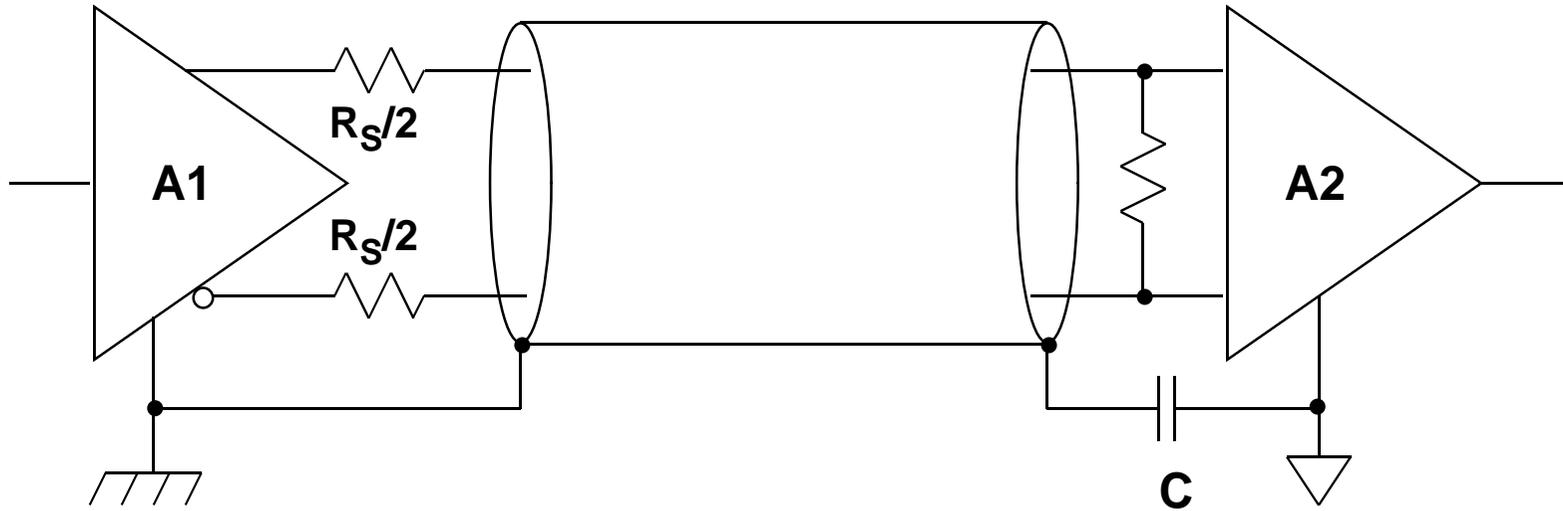


# GROUNDING SHIELDED CABLE WITH REMOTE PASSIVE SENSOR



a

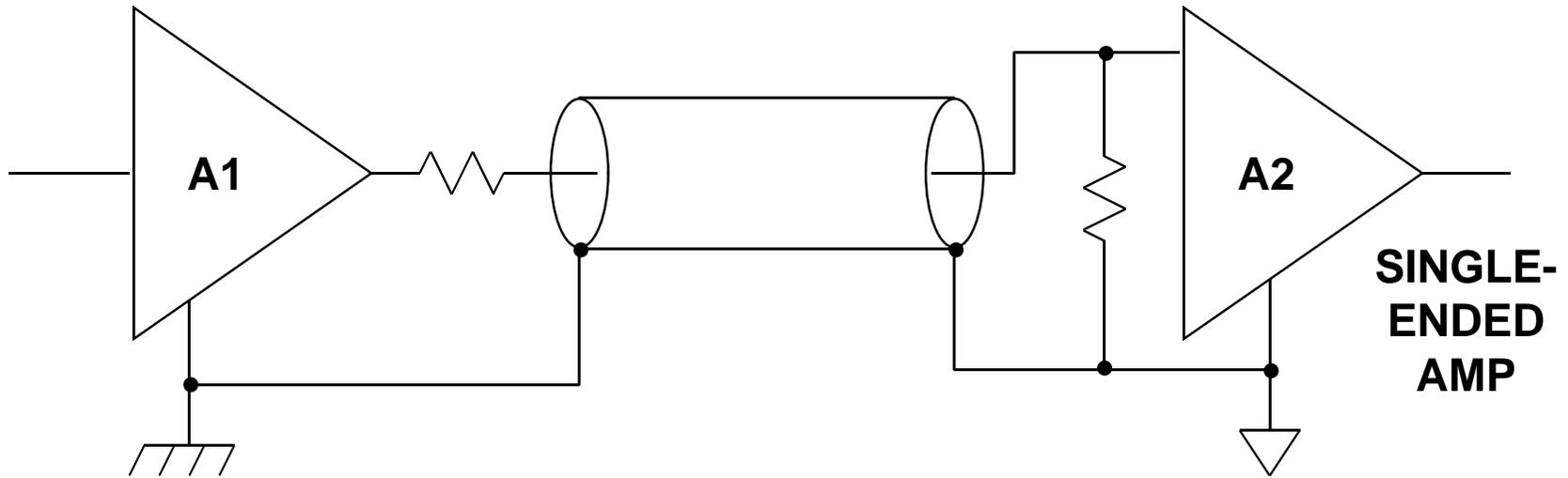
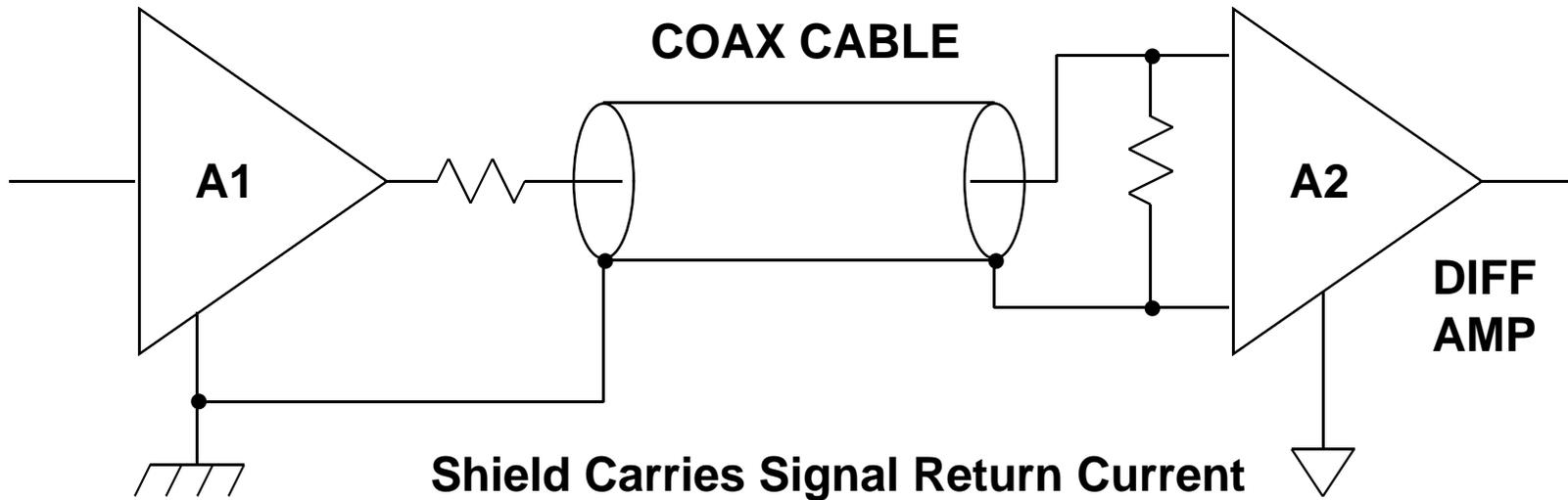
# GROUNDING SHIELDED CABLE WITH REMOTE ACTIVE SENSOR



a

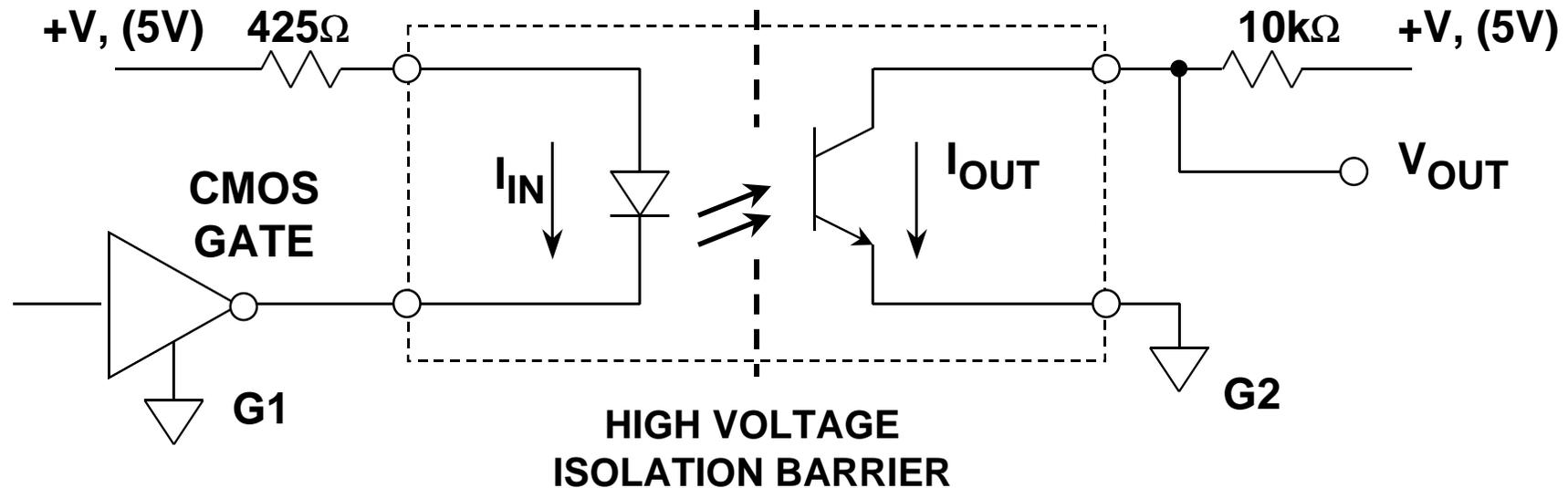
10.43

# COAXIAL CABLE GROUNDING



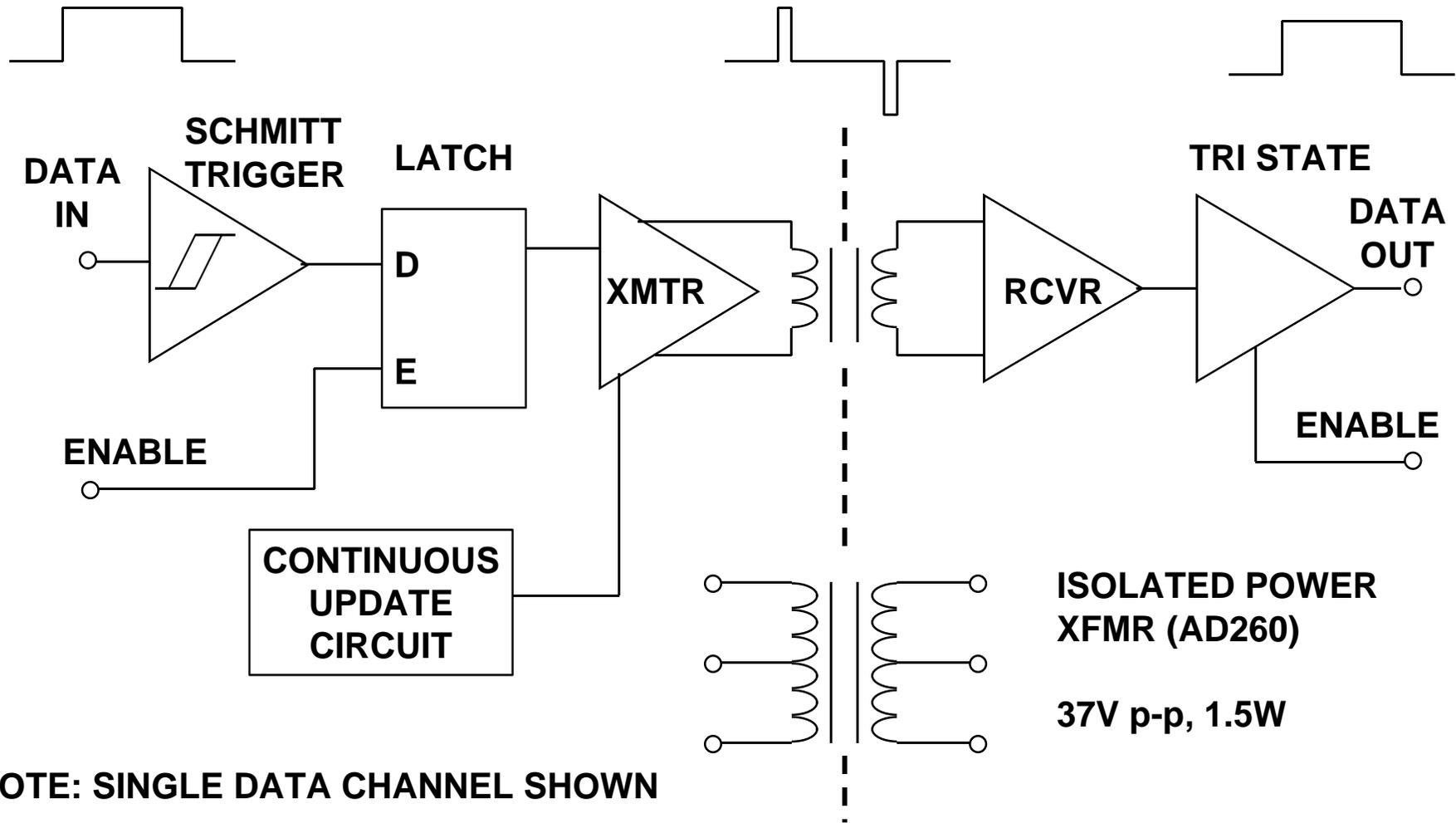
a

# ISOLATION USING OPTOISOLATORS



- Uses Light for Transmission Over a High Voltage Barrier
- The LED is the Transmitter, and the Phototransistor is the Receiver
- High Voltage Isolation: 5000V to 7000V
- Non-Linear -- Best for Digital or Frequency Information
- Rise and Fall-times can be 10 to 20μs in Slower Devices
- Example: Siemens IL-1 (<http://www.siemens.com>)

# AD260/AD261 DIGITAL ISOLATORS



NOTE: SINGLE DATA CHANNEL SHOWN

3.5kV RMS ISOLATION BARRIER  
(AD260B/AD261B)

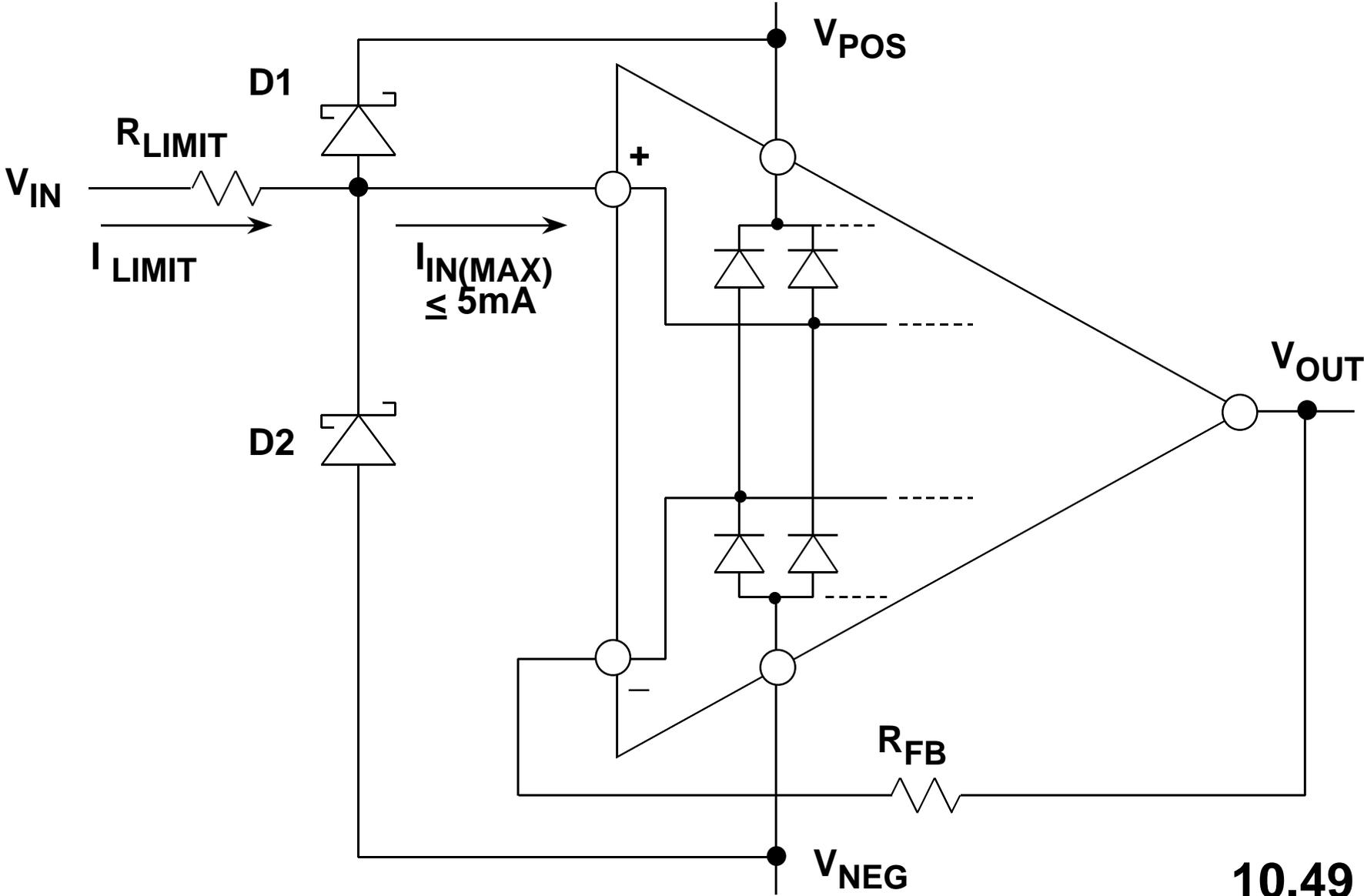
# AD260/AD261 DIGITAL ISOLATOR KEY SPECIFICATIONS

- Isolation Test Voltage to 3.5kV RMS (AD260B/AD261B)
- Five Isolated Digital Lines Available in 6 Input/Output Configurations
- Logic Signal Frequency: 20MHz Max.
- Isolated Power Transformer: 37V p-p, 1.5W (AD260)
- Waveform Edge Transmission Symmetry:  $\pm 1$ ns
- Propagation Delay: 14ns
- Rise and Fall-Times < 5ns

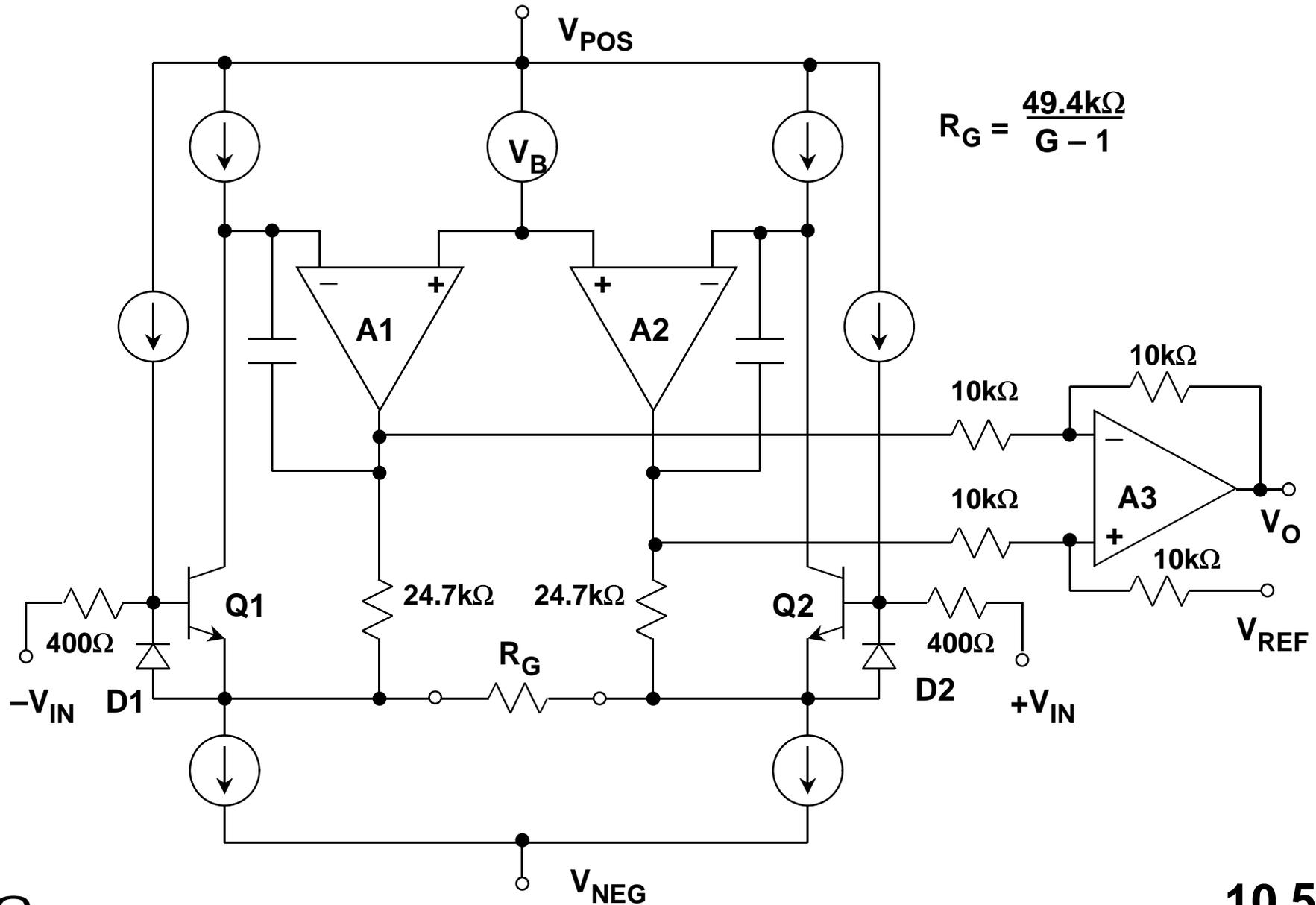
# INPUT OVERVOLTAGE

- **INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS**  
(Usually Specified With Respect to Supply Voltages)
- **A Common Specification Requires the Input Signal Remain Within 0.3V of the Supply Rails**
- **Input Stage Conduction Current Should Be Limited**  
(Rule of Thumb:  $\leq 5\text{mA}$  Unless Otherwise Specified)
- **Avoid Reverse Bias Junction Breakdown in Input Stage Junctions**
- **Differential and Common Mode Ratings May Differ**
- **No Two Amplifiers are Exactly the Same**
- **Some ICs Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still Be Observed**

# GENERALIZED EXTERNAL OVERVOLTAGE PROTECTION CIRCUIT FOR OP AMPS



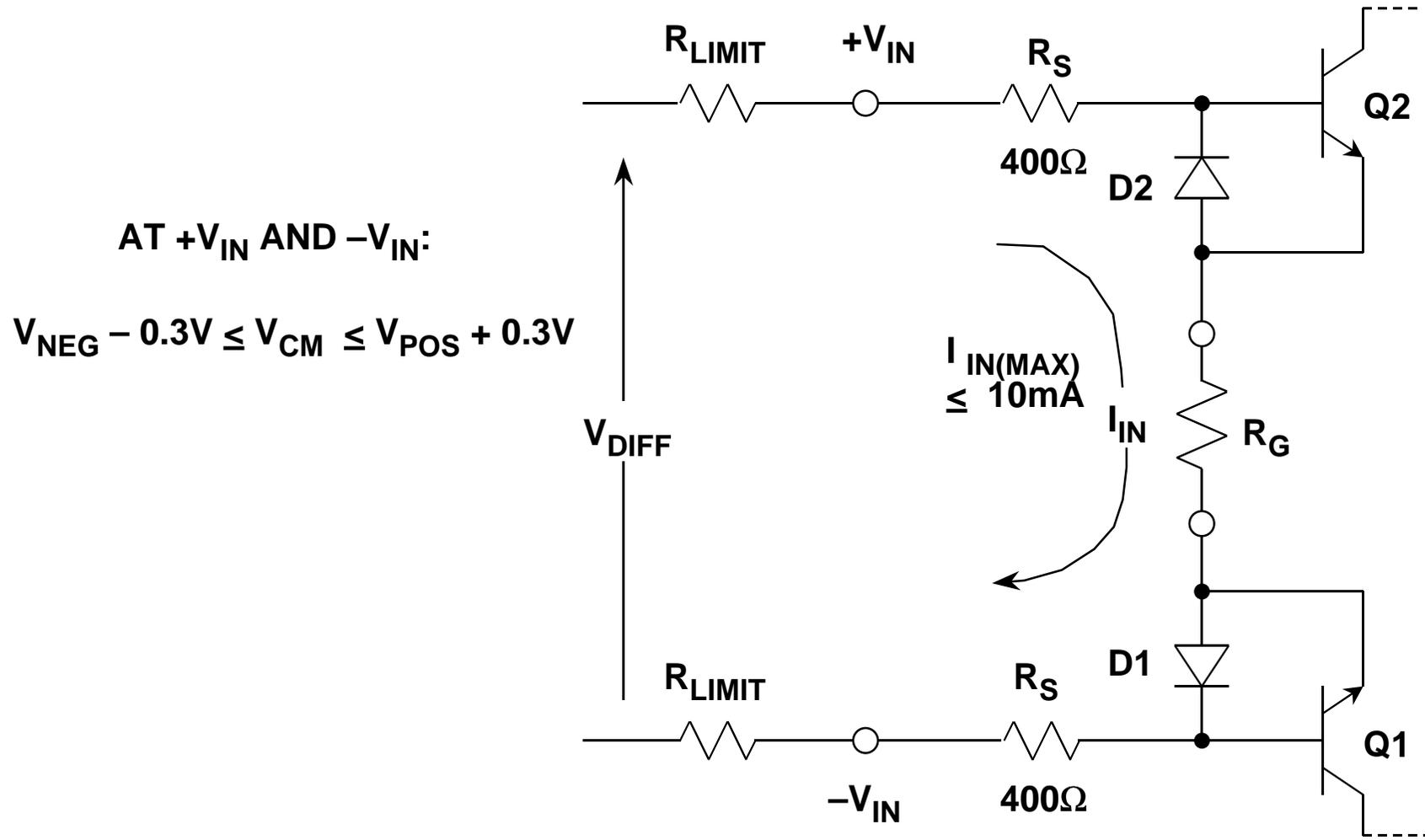
# AD620 SIMPLIFIED SCHEMATIC



a

10.50

# AD620 EQUIVALENT INPUT CIRCUIT WITH OVERVOLTAGE

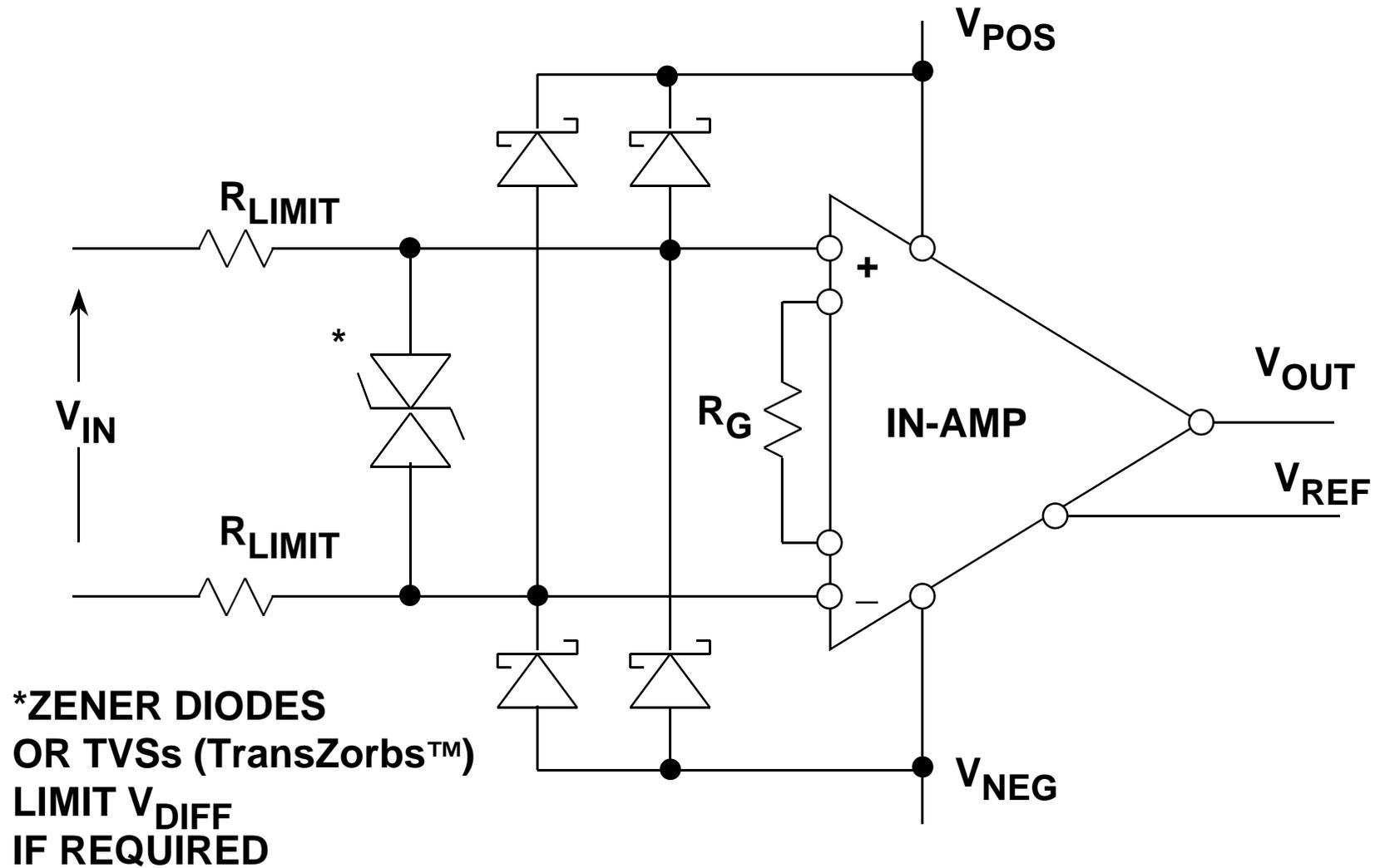


$$V_{DIFF} = I_{IN}(2R_S + 2R_{LIMIT} + R_G) + 1.2V$$

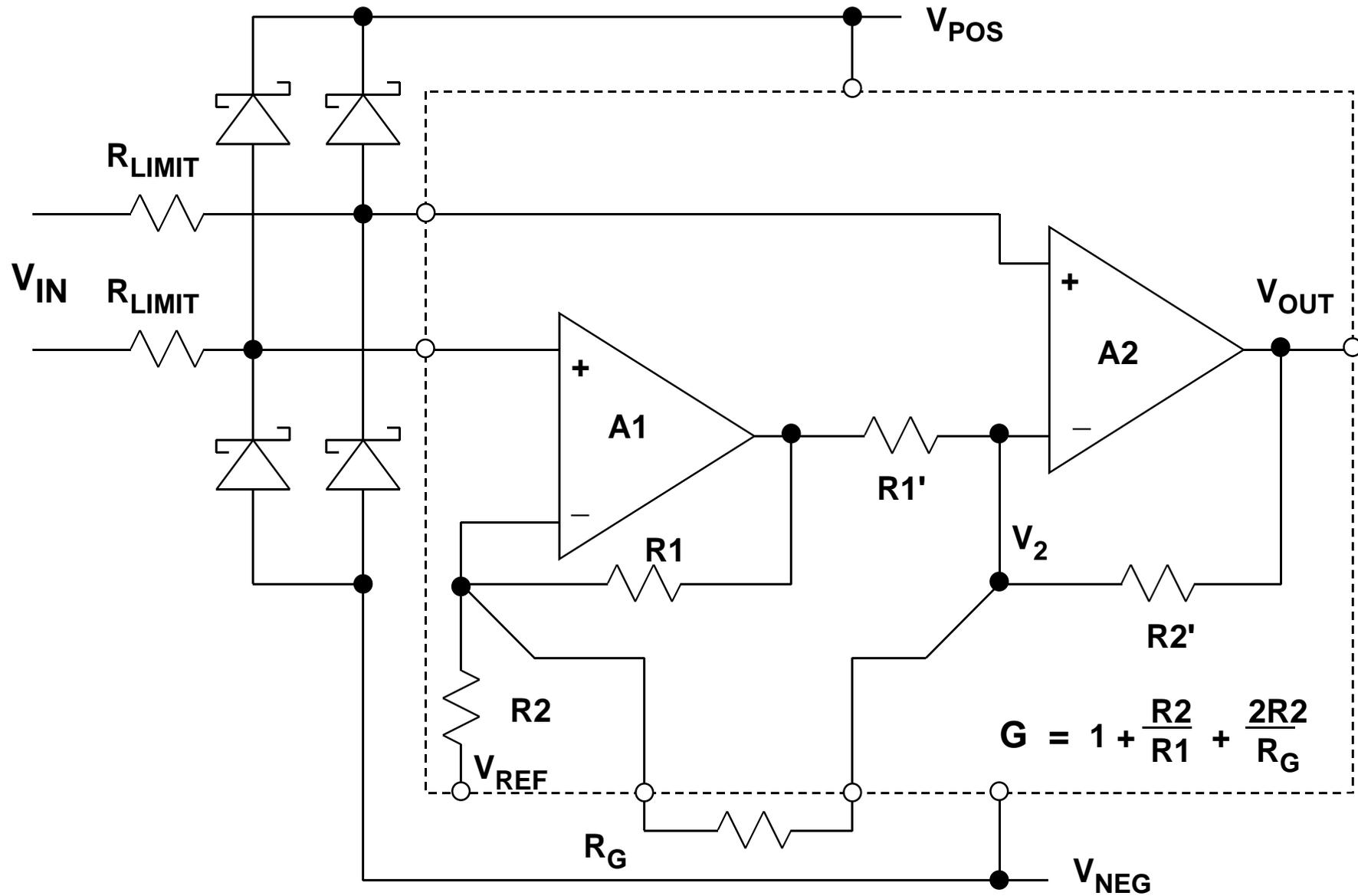
$$V_{DIFF(MAX)} \leq I_{IN(MAX)}(2R_S + 2R_{LIMIT} + R_G) + 1.2V$$

a

# GENERALIZED EXTERNAL PROTECTION FOR INSTRUMENTATION AMPLIFIER INPUTS



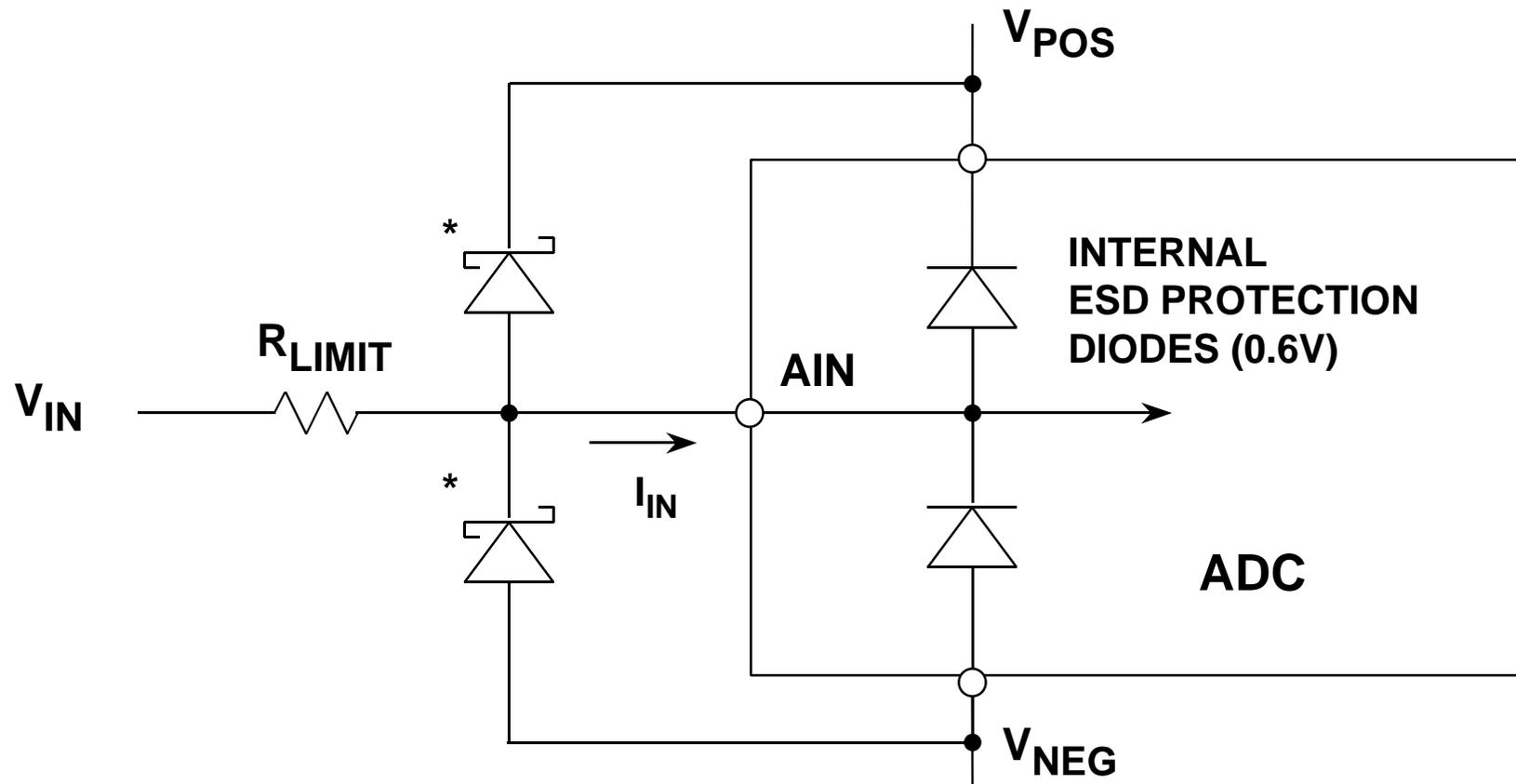
# INPUT PROTECTION FOR TWO OP AMP IN-AMP (AD627)



a

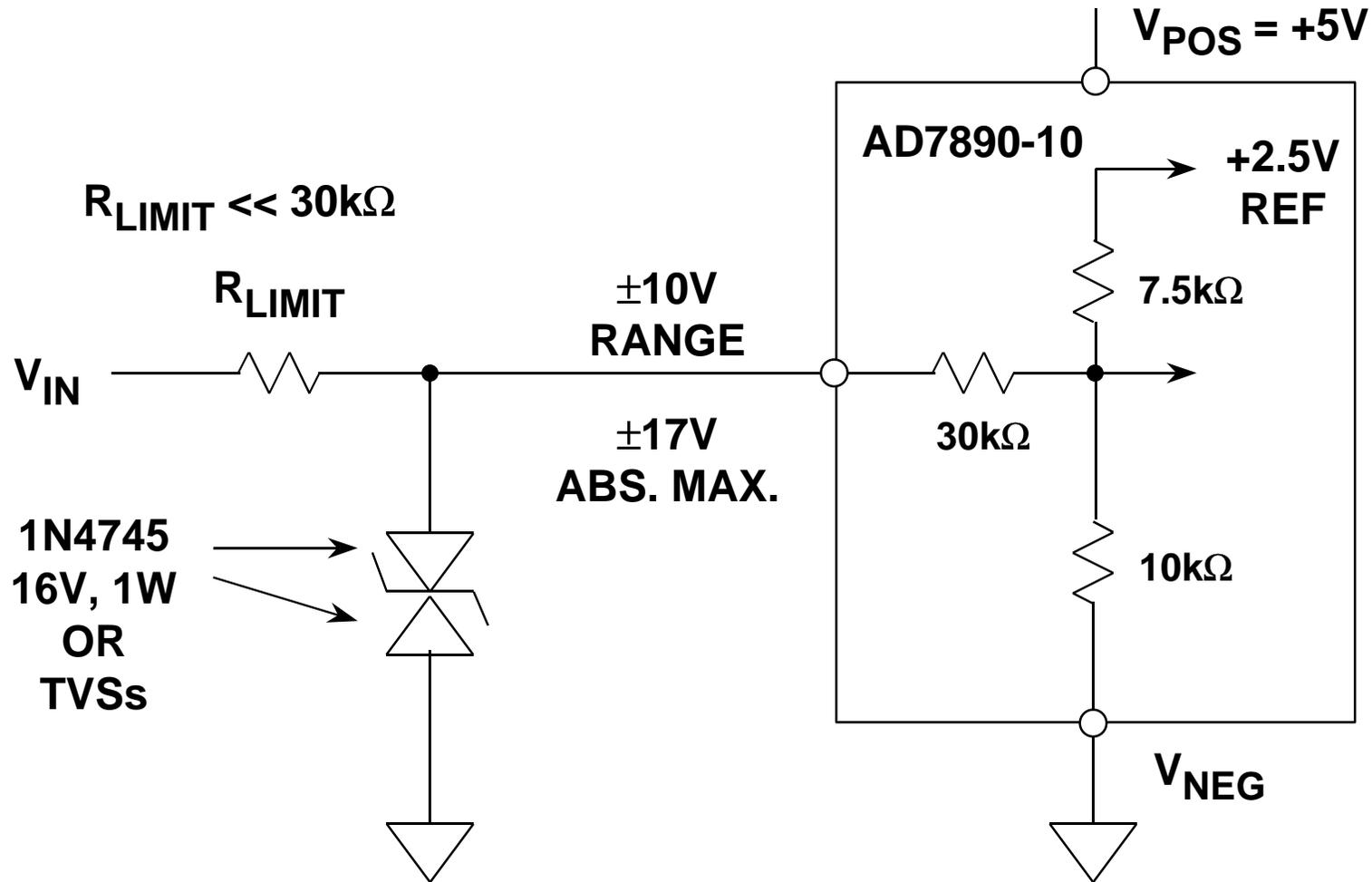
10.53

# INPUT PROTECTION FOR ADCs WITH INPUT RANGES WITHIN SUPPLY VOLTAGES

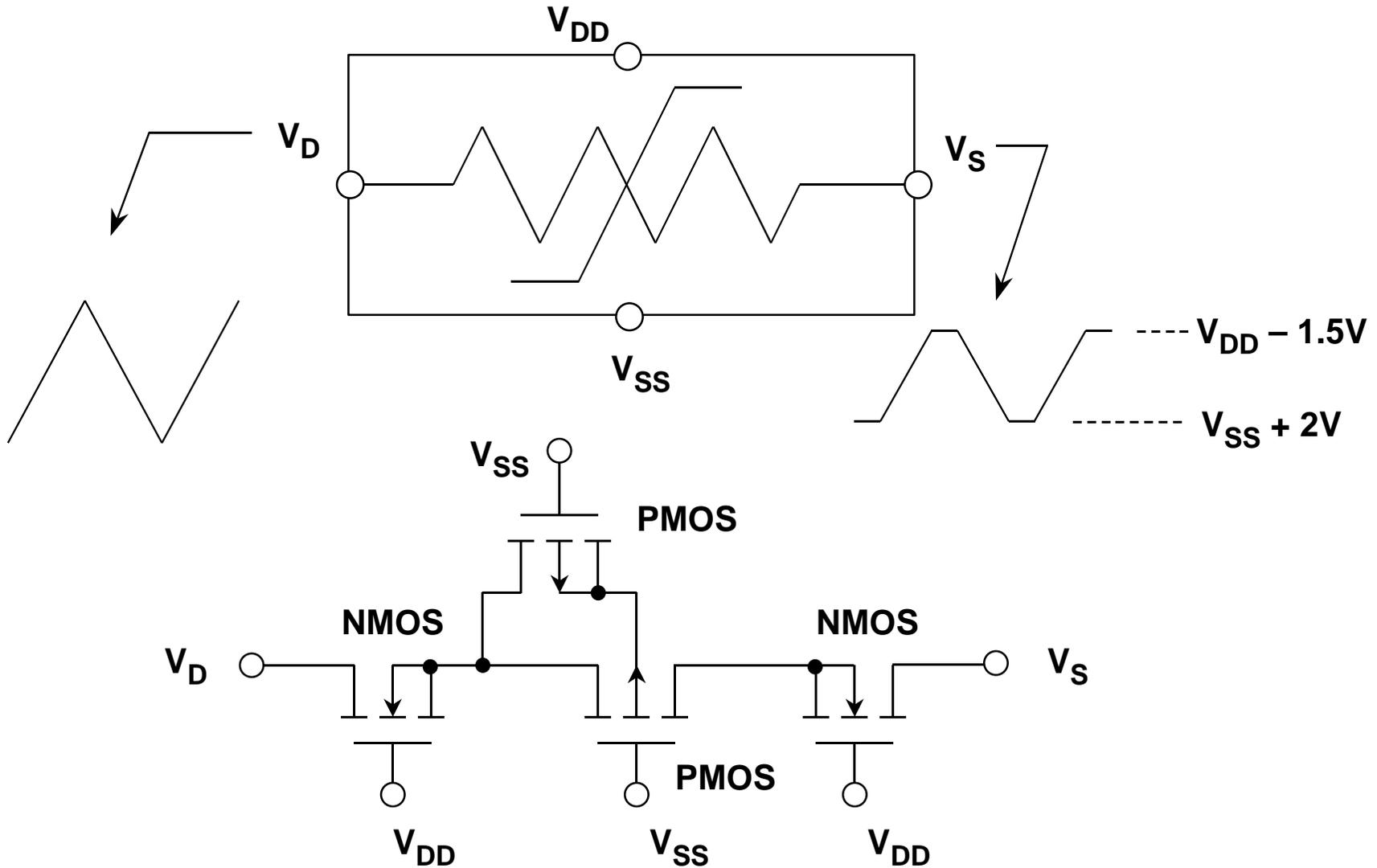


- Choose  $R_{LIMIT}$  to Limit  $I_{IN}$  Current to 5mA
- \*Additional External Schottky Diodes Allow Lower Values of  $R_{LIMIT}$

# INPUT PROTECTION FOR SINGLE-SUPPLY ADCs WITH THIN FILM RESISTOR INPUT ATTENUATORS



# ADG465, ADG466, and ADG467 SINGLE, TRIPLE, AND OCTAL CHANNEL PROTECTORS

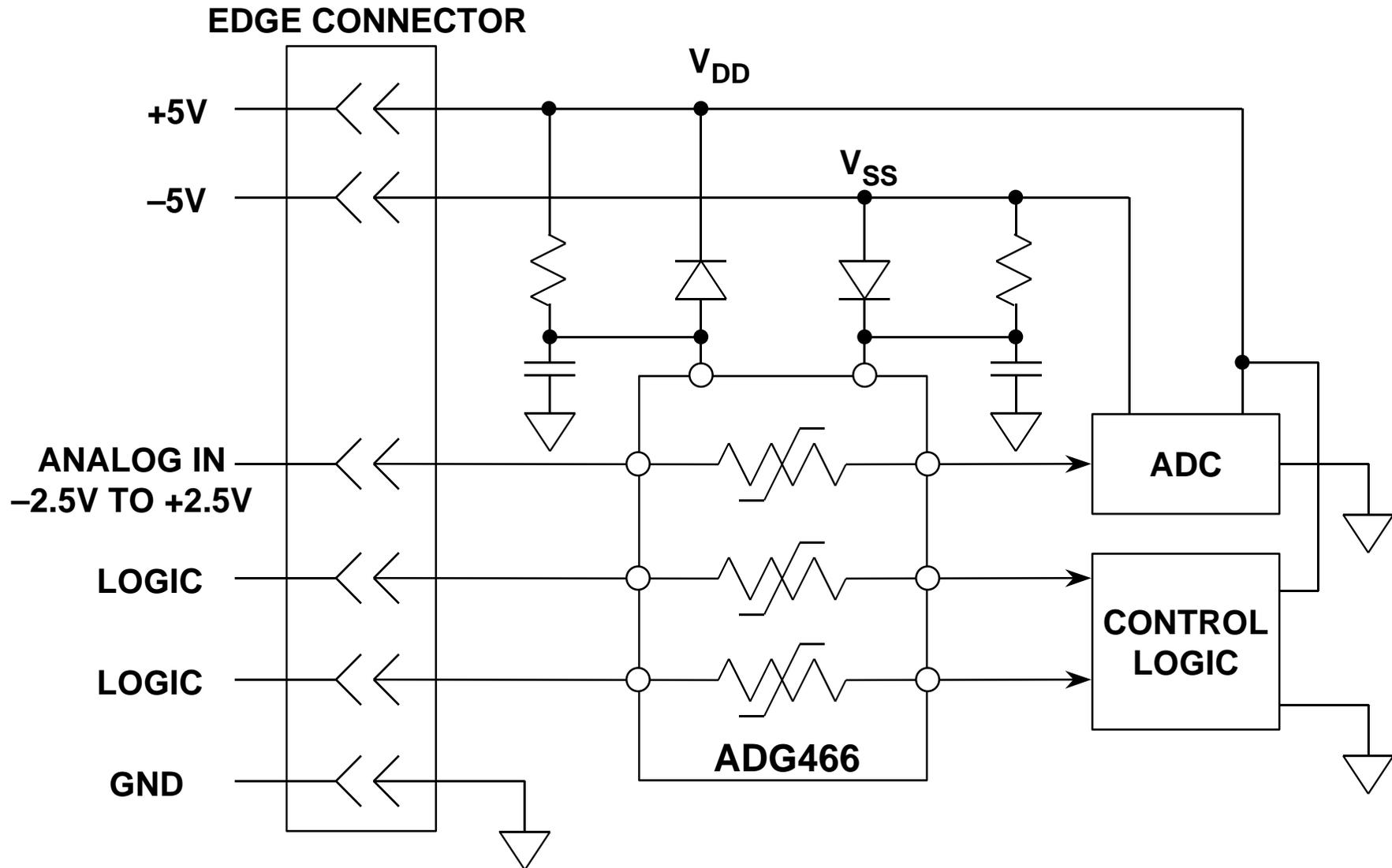


a

# ADG465, ADG466, and ADG467 CHANNEL PROTECTORS KEY SPECIFICATIONS

- Low On-Resistance (50Ω for ADG465, 80Ω for ADG466/467)
- On-Resistance Match: 3%
- 44V Maximum Supply Voltage,  $V_{DD} - V_{SS}$
- Fault and Overvoltage Protection up to  $\pm 40V$
- Positive Overvoltages Clamped at  $V_{DD} - 1.5V$
- Negative Overvoltages Clamped at  $V_{SS} + 2V$
- Signal Paths Open-Circuit with Power Off
- Latch-Up Proof Construction

# OVERVOLTAGE AND POWER SUPPLY SEQUENCING PROTECTION USING THE ADG466



a

10.58

# EXAMPLES OF ELECTROSTATIC CHARGE GENERATION

- **Walking Across a Carpet**
  - ◆ **1000V - 1500V Generated**
- **Walking Across a Vinyl Floor**
  - ◆ **150V - 250V Generated**
- **Handling Material Protected by Clear Plastic Covers**
  - ◆ **400V - 600V Generated**
- **Handling Polyethylene Bags**
  - ◆ **1000V - 2000V Generated**
- **Pouring Polyurethane Foam Into a Box**
  - ◆ **1200V - 1500V Generated**
- **Note: Assume 60% RH. For Low RH (30%), Generated Voltages Can Be >10 Times Those Listed Above**

# UNDERSTANDING ESD DAMAGE

## ■ ESD Failure Mechanisms:

- ◆ Dielectric or junction damage
- ◆ Surface charge accumulation
- ◆ Conductor fusing

## ■ ESD Damage Can Cause:

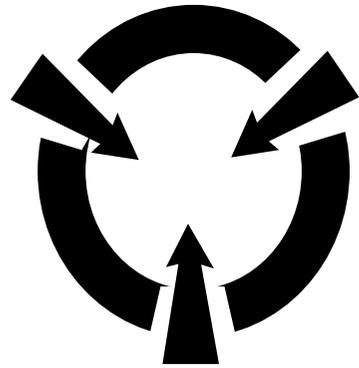
- ◆ Increased leakage
- ◆ Degradation in performance
- ◆ Functional failures of ICs.

## ■ ESD Damage is often Cumulative:

- ◆ For example, each ESD "zap" may increase junction damage until, finally, the device fails.

# RECOGNIZING ESD SENSITIVE DEVICES

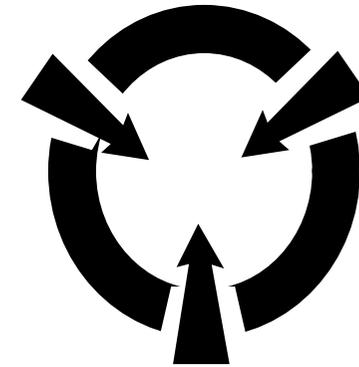
All static sensitive devices are sealed in protective packaging and marked with special handling instructions



**CAUTION**

**SENSITIVE ELECTRONIC DEVICES**

**DO NOT SHIP OR STORE NEAR STRONG  
ELECTROSTATIC, ELECTROMAGNETIC,  
MAGNETIC, OR RADIOACTIVE FIELDS**

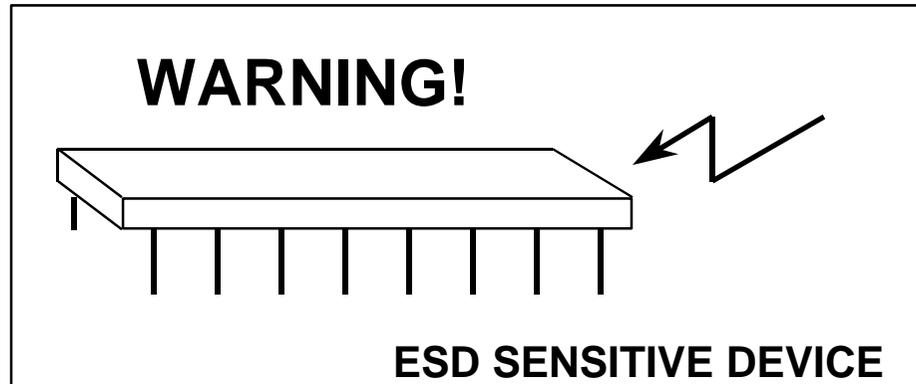


**CAUTION**

**SENSITIVE ELECTRONIC DEVICES**

**DO NOT OPEN EXCEPT AT  
APPROVED FIELD FORCE  
PROTECTIVE WORK STATION**

## ESD STATEMENT ON DATA SHEETS OF MOST LINEAR AND MIXED-SIGNAL ICs



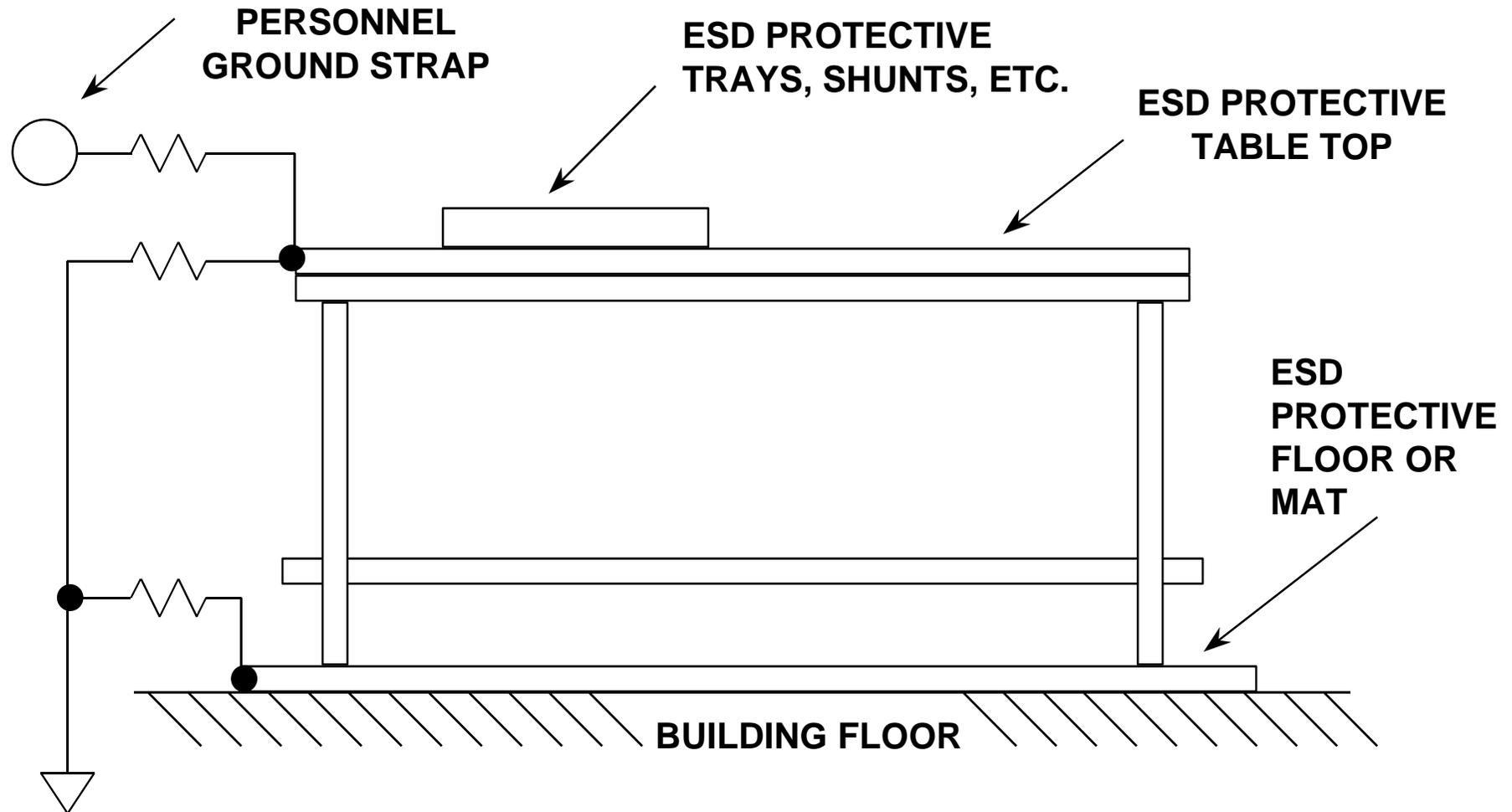
### CAUTION

---

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXXX features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

---

# WORKSTATION FOR HANDLING ESD-SENSITIVE DEVICES



Note: Conductive Table Top Sheet Resistance  $\approx 1\text{M}\Omega / \square$

a

10.63

# ESD PROTECTION REQUIRES A PARTNERSHIP BETWEEN THE IC SUPPLIER AND THE CUSTOMER

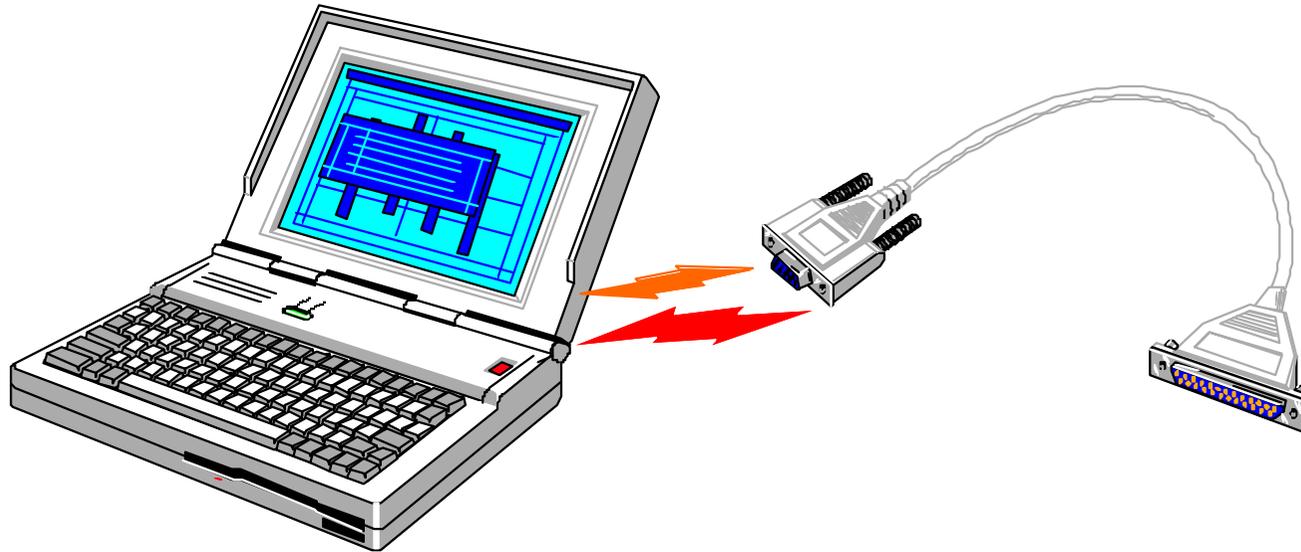
## ANALOG DEVICES:

- **Circuit Design and Fabrication -**
  - ↓ Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.
  - ↓
- **Pack and Ship -**
  - ↓ Pack in static dissipative material. Mark packages with ESD warning.

## CUSTOMERS:

- **Incoming Inspection -**
  - ↓ Inspect at grounded workstation. Minimize handling.
- **Inventory Control -**
  - ↓ Store in original ESD-safe packaging. Minimize handling.
- **Manufacturing -**
  - ↓ Deliver to work area in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.
  - ↓
- **Pack and Ship -**
  - ↓ Pack in static dissipative material if required. Replacement or optional boards may require special attention.

## RS-232 PORT IS VERY SUSCEPTIBLE TO ESD



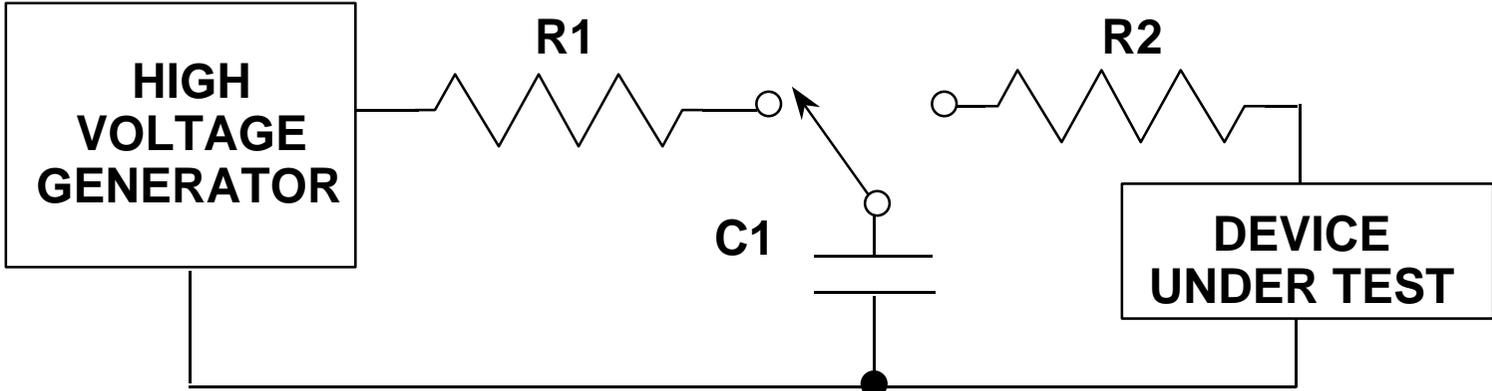
- I-O Transceiver Is Directly in the Firing Line for Transients - RS-232 Port Is Particularly Vulnerable
- I-O Port Is an Open Gateway in the Enclosure
- Harmonised Standards Are Now Mandatory Requirements in European Community

# IEC 1000-4-x BASIC IMMUNITY STANDARDS FOR ELECTRONIC EQUIPMENT (NOT ICs!)

- IEC1000-4 Electromagnetic Compatibility EMC
- IEC1000-4-1 Overview of Immunity Tests
- IEC1000-4-2 Electrostatic Discharge Immunity (ESD)
- IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity
- IEC1000-4-4 Electrical Fast Transients (EFT)
- IEC1000-4-5 Lightning Surges
- IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz
- Compliance Marking:



# MIL STD 883B METHOD 3015.7 HUMAN BODY MODEL VERSUS IEC 1000-4-2 ESD TESTING

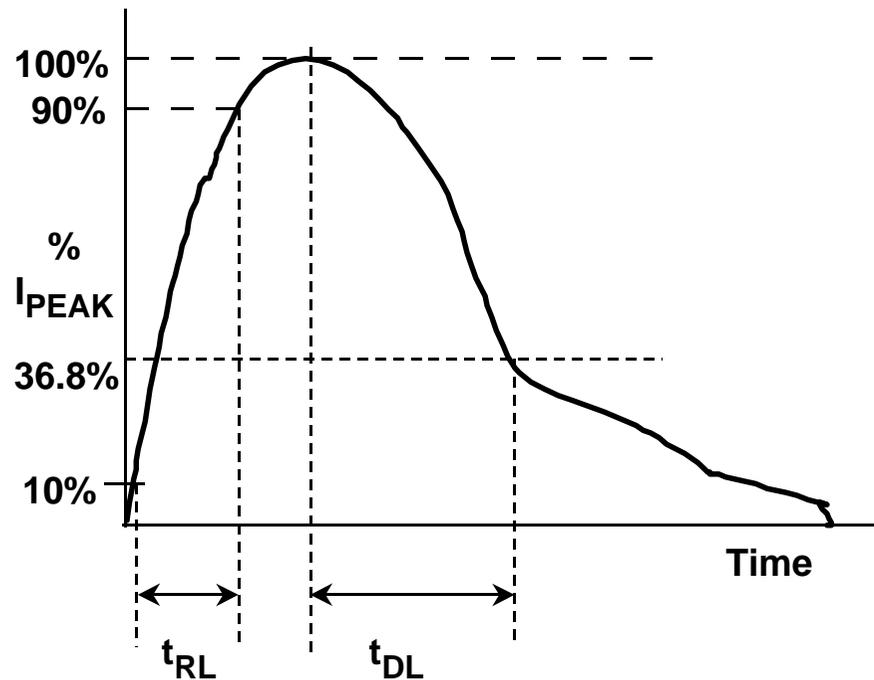


ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

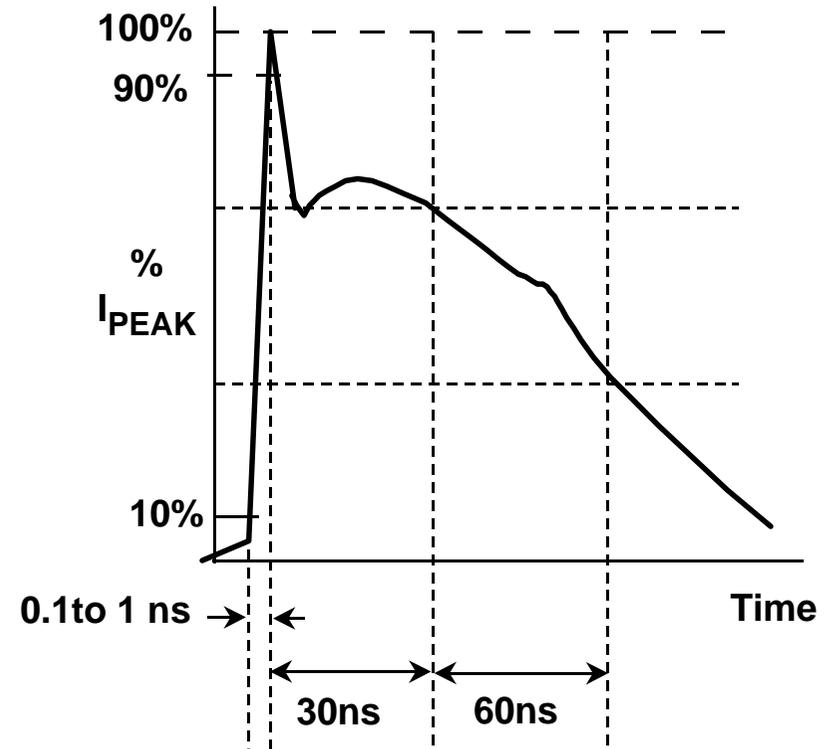
**NOTE: CONTACT DISCHARGE VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV**

# MIL-STD-883B, METHOD 3015.7 HUMAN BODY MODEL AND IEC 1000-4-2 ESD WAVEFORMS

**HUMAN BODY MODEL  
MIL-STD-883B, METHOD 3015.7**



**IEC 1000-4-2**



■ Voltage : 8 kV

■ Peak Current :

◆ MIL-883B, Method 3015.7 HBM : 5 A

◆ IEC 1000-4-2 : 25 A

# **CUSTOMER DESIGN PRECAUTIONS FOR ICs WHICH MUST OPERATE AT ESD-SUSCEPTIBLE INTERFACES**

- **Observe all Absolute Maximum Ratings on Data Sheet!**
- **Follow General Overvoltage Protection Recommendations**
  - ◆ **Add Series Resistance to Limit Currents**
  - ◆ **Add Zeners or Transient Voltage Suppressors (TVS) TransZorbs™ for Extra Protection (<http://www.gensemi.com>)**
- **Purchase ESD-Specified Digital Interface Devices Such as**
  - ◆ **ADMXXX-E Series of RS-232 / RS-485 Drivers / Receivers (MIL-883B, Method 3015.7: 15kV, IEC 1000-4-2: 8kV)**
- **Read AN-397, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence," by Niall Lyne - Available from Analog Devices, <http://www.analog.com>**